Semiconductors@Purdue

FALL 2024

PURDUE UNIVERSITY

For more information on Semiconductors at Purdue, please visit our website at:
https://engineering.purdue.edu/semiconductors

or email Cristina Farmus at:
cfarmus@purdue.edu or semiconductors@purdue.edu

Cover photo:

SK hynix semiconductor advanced packaging investment in Purdue Research Park announcement, April 2024.

(Photo Credit: Purdue Marketing and Communications)

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Semiconductors@Purdue

Purdue University is uniquely positioned to offer a full range of options for partners interested in semiconductors and microelectronics: research and innovation, workforce and talent, and business growth. As a top 10 public university in the U.S. that moves fast and gets things done, Purdue pursues excellence at scale, with the largest engineering college (over 16,000 engineering students) ever ranked among the top 5 in the U.S and top 5 university in the world in receiving U.S. patents.

Purdue University is home to large scale, impactful, interdisciplinary research and learning in semiconductors. A strong, critical mass of researchers sets Purdue apart by spanning the full stack of semiconductors R&D from materials and devices, to circuits, systems, architecture, and advanced packaging integration. Purdue currently leads three and participates in two Semiconductor Research Corporation funded multi-university research programs. Strong connections to industry, such as DoD, Commerce/NIST, and NSF, support one of the nation's largest and best semiconductors research programs.

Purdue's reputation as an R&D trailblazer is matched by its leadership in workforce development. In May 2022, we launched the Semiconductor Degrees Program, a full suite of degrees and credentials options for semiconductors education, ranging from on-campus courses to a new set of degrees, competitive internships, innovative Learning While Working program, flexible online courses, and virtual lab. Purdue leads the Scalable Asymmetric Life Cycle Engagement (SCALE), a five-year, DoD sponsored national coalition of 19 universities aimed at addressing the urgent need to develop a highly skilled U.S. microelectronics workforce to bolster national security.

In 2023, Purdue announced four like-minded global partnerships in semiconductor workforce and innovation. Purdue signed an agreement to become the flagship academic partner for the government of India, establishing Purdue as a key collaborator with the India Semiconductor Mission (ISM). As announced at the G7 meeting in May 2023 in Japan, Purdue University hosted the inaugural meeting of the UPWARDS Network for workforce advancement, and research and development in semiconductors, led by Micron and Tokyo Electron, with 11 U.S. and Japanese universities forming a partnership, along with the U.S. National Science Foundation. On June 19, Purdue and TSMC renewed the partnership in the Center for Secure Microelectronics Ecosystems. In December 2023, Purdue University and Belgium-based technological innovation organization imec celebrated the grand opening of a research and development hub at the Convergence Center for Innovation and Collaboration at Purdue's campus. The presence of imec at Purdue will help facilitate groundbreaking advancements in semiconductor technologies.

On April 3rd, 2024 we celebrated the announcement that SK hynix Inc., the world's sixth-largest semiconductor company, will build a semiconductor manufacturing facility at Purdue Research Park in West Lafayette, Indiana.

As part of Purdue@DC, the full-day CHIPS for America: Execute for Success 2023 Policy and Strategy Summit, held at the Russell Senate Office Building in April, 2023, convened hundreds of attendees representing over 175 entities from over 23 states, and focused on strategies to execute the vision outlined in CHIPS for America: Vision for Success. Featuring a fireside keynote with Secretary Gina Raimondo and Senator Todd Young, the Summit highlighted the implementation of federal investments and future policy actions and facilitated the creation of government, industry, and academic partnerships. We are planning the CHIPS for America: Execute for Global Success 2024 Policy and Strategy Summit on April 17th, 2024, at the same location, and we invite you to join us as we focus on U.S. competitiveness in semiconductor R&D and workforce in a global context.

> “Semiconductor excellence at scale runs deep within the DNA of Purdue. From the invention of MOSFET by Mohamed Atalla, a proud Boilermaker engineer, to the creation of the Silicon Valley by Fred Terman who hailed from the Hoosier soil. Today, Purdue is America’s semiconductor university, where cutting-edge research, workforce development, and “lab-to-fab” collaboration with industry converge. With over 50 esteemed faculty in the nation’s top 4 engineering college, we have launched the first comprehensive Semiconductor Degrees Program, welcomed European technology leader imec to campus with the grand opening of a research and development hub, established Purdue as a key collaborator with India Semiconductor Mission, and signed the U.S.-Japan semiconductor agreement at the G7 summit. Together with the state of Indiana and Navy Crane, and leading with actions on national policies in Washington D.C., Purdue is the heart of the Silicon Crossroads.”

Mung Chiang

President

Roscoe H. George Distinguished Professor, Elmore Family School of Electrical and Computer Engineering

Purdue University

Mark Lundstrom

Senior Advisor to the President and Chief Semiconductor Officer

Don and Carol Scifres Distinguished Professor, Elmore Family School of Electrical and Computer Engineering

Purdue University

2022
- MAY → Purdue launches Semiconductor Degrees Program
- AUG → CHIPS and Science Act enacted
- OCT → Purdue establishes semiconductor degrees leadership board

2023
- APR → CHIPS for America: Execute for Success Policy and Strategy Summit
- MAY → Purdue-imec partnership announced
- → Purdue and India semiconductor alliance announced
- → Purdue signs landmark UPWARDS U.S.–Japan agreement in semiconductors at G7 summit
- → Purdue Summer Training, Awareness, and Readiness for Semiconductors (STARS) commences
- JUN → Purdue, TSMC extend partnership on semiconductor research and workforce development
- → Purdue becomes founding partner in SEMI Midwest chapter
- → High School READI program commences
- SEP → Purdue establishes permanent presence next to NSWC Crane for future of national defense and semiconductors
- OCT → Purdue University Silicon Summit
- DEC → imec opens innovation hub at Purdue

2024
- FEB → Purdue-Dassault Systèmes Partnership to improve, accelerate, and transform semiconductor workforce development
- APR → CHIPS for America: Execute for Global Success Summit
- → SK hynix announces fab at Purdue
- MAY → Purdue STARS Program Year Two Begins
- JUN → Purdue–Ivy Tech Chips Program (PITCH) Year Two Begins
- OCT → SEMI Midwest Meeting at Purdue

2025
- APR → SEMIEXPO in the Heartland in Indianapolis

Purdue President's CHIPS Act Capture Task Force

An expanded Purdue University taskforce devoted to semiconductors and microelectronics has reasserted the university's focus on helping the U.S. regain preeminence in the industry. Leading the taskforce is Mark Lundstrom, as Chief Semiconductor Officer for Purdue and Senior Advisor to President Mung Chiang.

The President's Semiconductor Taskforce will coordinate and lead Purdue's efforts toward innovative research and development through the CHIPS for America and Science Act, approved in 2022 in Washington, D.C. The taskforce will consist of faculty experts from several areas of Purdue microelectronics. Purdue expanding semiconductor research and development already runs the gamut of disciplines in the field, from materials and devices to circuits, systems, architecture, and advanced packaging integration. Strong connections in industry, defense, and the National Science Foundation further support Purdue's research.

Mark Lundstrom | Taskforce Leader

Senior Advisor to the President; Chief Semiconductor Officer; Don and Carol Scifres Distinguished Professor, Elmore Family School of Electrical and Computer Engineering

Joerg Appenzeller

Scientific Director of Nanoelectronics, Birck Nanotechnology Center; Barry M. and Patricia L. Epstein Professor, Elmore Family School of Electrical and Computer Engineering

Muhammad Ashraf Alam

Jai N. Gupta Distinguished Professor of Electrical and Computer Engineering, Elmore Family School of Electrical and Computer Engineering

Peter Bermel

Director of SCALE; Associate Director of Graduate Admissions; Elmore Professor, Elmore Family School of Electrical and Computer Engineering

Zhihong Chen

Mary Jo and Robert L. Kirk Director, Birck Nanotechnology Center; Reilly Professor, Elmore Family School of Electrical and Computer Engineering

Cristina Farmus

Vice President, Special Projects;
Interim Vice President, Industry Partnerships

Anand Raghunathan

Silicon Valley Professor of Electrical and Computer Engineering, Elmore Family School of Electrical and Computer Engineering

Vijay Raghunathan

Vice President for Global Partnerships and Programs; Director of Semiconductor Education; Professor of Electrical and Computer Engineering, Elmore Family School of Electrical and Computer Engineering

Kaushik Roy

Director, Center for Brain-Inspired Computing, a DARPA/SRC JUMP Center; Edward G. Tiedemann Jr. Distinguished Professor, Elmore Family School of Electrical and Computer Engineering

Ganesh Subbarayan

Co-director, SRC Center for Heterogeneous Integration Research in Packaging;
James G. Dwyer Professor of Mechanical Engineering, School of Mechanical Engineering

Silicon Crossroads Hub:
Purdue's Semiconductor Innovation Ecosystem Grows with CHIPS-Funded, Indiana-Led Semiconductor Hub

OCTOBER 17, 2023

Submitted through the Applied Research Institute, the Indiana-led proposal "Silicon Crossroads" was announced September 20 by the Department of Defense as one of eight Microelectronics Commons Hubs selected out of over 80 proposals across the U.S. The Naval Surface Warfare Center, Crane Division (NSWC Crane), in Indiana will manage the program.

The hubs are the first major program funded through the CHIPS and Science Act 2022, co-sponsored by U.S. Sen. Todd Young of Indiana. The total five-year budget is around $2 billion; FY23 is year 1 and has a budget of $238 million. The Indiana-led consortium, with participation from Illinois and Michigan, received $33 million as part of the year 1 budget and is the largest hub in the Midwest.

"As we collectively work to grow the nation's microelectronics base, Indiana will play a key role in the development of these critical national security technologies and capabilities," Young said. "More broadly, this announcement shows how the CHIPS and Science Act will connect more of America, including the industrial Midwest, to the innovation economy."

Indiana leads the Silicon Crossroads Hub, and as its leading university Purdue will collaborate with many members of the consortium in the coming years. Purdue is a national leader in microelectronics materials, devices, chip design, tool development, manufacturing, packaging and sustainability, spanning the semiconductor ecosystem in software and hardware with long-standing faculty excellence.

> *"Located in America's heartland, Silicon Crossroads builds on the Midwest's strengths in research and development as well as workforce training at all levels to build a domestic semiconductor industry—a national security imperative to keep our nation ahead of our adversaries."*
>
> **Eric Holcomb,** Indiana Governor

CHIPS for America: Execute for Global Success

APRIL 17, 2024

More than 330 representatives from industry, government, and academia gathered in person and online Wednesday, April 17th, 2024 in Washington, D.C., as Purdue University and an alliance of industry partners hosted the daylong CHIPS for America: Execute for Global Success summit at the Russell Senate Office Building.

The summit—a collaborative event held by SEMI, Semiconductor Industry Association, Semiconductor Research Corporation, Global Semiconductor Alliance, and Purdue—attracted a dynamic coalition of global allies as well as industry and academic stakeholders to examine wide-ranging solutions at scale to address the future of U.S. innovation in microelectronics and the semiconductor workforce.

Purdue President Mung Chiang and Indiana Senator Todd Young during their Fireside Chat at the CHIPS Summit.

(Photo: Kelsey Lefever, Purdue University)

Dr. Arati Prabhakar, Director, White House Office of Science and Technology Policy and Assistant to the President for Science and Technology, delivering a keynote title "How the Biden-Harris Administration is Advancing U.S. Semiconductor R&D."

(Photo: Kelsey Lefever, Purdue University)

Now in its second year in the nation's capital, the chip-focused conference created an opportunity to discuss research and development collaboration, workforce development opportunities, and supply chain partnerships in the semiconductor ecosystem.

Attendees represented 21 like-minded partners from the Asia-Pacific region, Europe, Central and South America, and industry, academic, and government organizations from 26 states and Washington, D.C.

Ambassadors and other high-ranking government officials from India, Japan, and Taiwan addressed the summit as part of three discussion panels.

Representatives from Belgium, Costa Rica, the Dominican Republic, France, Germany, the Netherlands, Panama, Peru, Romania, South Korea, Singapore, and the United Kingdom participated in the conference.

The Honorable Ramin Toloui, Assistant Secretary for the Bureau of Economic and Business Affairs, U.S. Department of State introducing the International Semiconductors Landscape Panel.

(Photo: Kelsey Lefever, Purdue University)

SK hynix Inc. CEO Kwak Noh-Jung delivering a keynote addressing and recognizing the importance of international collaboration, especially with the U.S., to enhance the semiconductor industry's resilience, foster innovation and advance supply chain sustainability.

(Photo: Kelsey Lefever, Purdue University)

CHIPS for America: Execute for Global Success *(cont'd)*

APRIL 17, 2024

PANEL:

International Semiconductors Landscape

Moderated by:
the Honorable Ramin Toloui

(Photo: Kelsey Lefever, Purdue University)

Left to right:

Hideaki Fujisawa, *Economic Minister, Embassy of Japan in the U.S.*

Alexander Tah-Ray Yui, *Representative to the U.S., Taipei Economic and Cultural Representative Office*

Dr. Ajay Kumar, *Minister of Commerce, Embassy of Indiana to the U.S.*

PANEL:

Global R&D Partnerships: Opportunities and Challenges

Moderated by:
Mark Lundstrom, Chief Semiconductor Officer, Purdue University

(Photo: Kelsey Lefever, Purdue University)

Left to right:

Richard-Duane Chambers, *Director of Policy and Integration, CHIPS R&D Office*

Matt Nicholls, *Vice President, Government Programs and Business Development, IBM Research*

Dr. Shadi Sandvik, *Senior Vice Chancellor for Research, Innovation, and Economic Development and Professor of Nanoscale Engineering, State University of New York*

Raj Jammy, *President, U.S. Operations, imec*

Dr. Philip Wong, *Willard R. Inez Kerr Bell Professor in the School of Engineering, Stanford University and Chief Scientist, TSMC, in a consulting, advisory role*

What Purdue Offers

#4
BEST ENGINEERING GRADUATE SCHOOL IN THE U.S.
U.S. News & World Report, 2023-24

#8
TOP U.S. PUBLIC UNIVERSITY
QS World University Ranking

#4
IN THE U.S. FOR PATENTS
U.S. Patent and Trademark Office, 2023

#1 OUT OF 15
SAFEST COLLEGE TOWN
Academic Influence

TOP 10 Most Innovated UNIVERSITY IN AMERICA 5 YEARS RUNNING *U.S. News & World Report, 2023*

- Advanced Research & Development facilities with more than 400 research labs on the West Lafayette campus, including the Scifres Nanotechnology Laboratory, the second largest clean room in academia.
- Advanced Packaging and Heterogeneous Integration, novel approaches to information, emerging memory technologies, reliability, and sustainability of electronics.
- Exceptional faculty with 23 members of the National Academy of Engineering.
- Innovative faculty and staff with 18 National Academy of Inventors Fellows at Purdue, of which 14 are in the College of Engineering.
- A pipeline of globally competitive talent needed to innovate and thrive with over 11,000 engineering undergraduate and 4,000 graduate students.
- A business-minded university with an interwoven business and social ecosystem, backed by Purdue Research Foundation track record of meeting industry partners' needs with space, logistics, and community connections.

NOTABLE PURDUE RANKINGS

RANKING	SOURCE	NATION
Engineering Graduate Program	U.S. News & World Report	#4
Engineering Undergraduate Program	U.S. News & World Report	#9
Online Graduate Engineering Program	U.S. News & World Report	#2
Most Innovative School	U.S. News & World Report	#7
Top U.S. Public University	The Wall Street Journal / Times Higher Education	#8
Best Value University	The Wall Street Journal / Times Higher Education	#7
Best University for Engagement	The Wall Street Journal / Times Higher Education	#1
University with Most Utility Patents in the World	U.S. Patent and Trademark Office	#4
Graduating the Most STEM Majors	Forbes	#5
Best Colleges for Veterans	College Consensus	#7
Safest College Town	SafeWise.com	#1
Best Online Learning School	Newsweek	#3

SK hynix Announces Facility for AI Memory Chips in Greater Lafayette

APRIL 3, 2024

SK hynix Inc. announced in April that it plans to invest close to $4 billion to build an advanced packaging fabrication and R&D facility for AI products in the Purdue Research Park. The development of a critical link in the U.S. semiconductor supply chain in West Lafayette marks a giant leap forward in the industry and the state. The new facility—home to an advanced semiconductor packaging production line that will mass-produce next-generation high-bandwidth memory, or HBM chips, the critical component of graphic processing units that train AI systems such as ChatGPT—is expected to provide more than a thousand new employment opportunities in the Greater Lafayette community. The company plans to begin mass production in the second half of 2028.

The project marks SK hynix's intention for long-term investment and partnership in Greater Lafayette. The company's decision-making framework prioritizes both profit and social responsibility while promoting ethical actions and accountability. From infrastructure developments that make accessing amenities easier to community empowerment projects such as skill development and mentorship, the SK hynix advanced packaging fabrication marks a new era of collaborative growth. The Biden-Harris Administration announced that the U.S. Department of Commerce and SK hynix have signed a non-binding preliminary memorandum of terms (PMT) to provide up to $450 million in proposed federal incentives under the CHIPS and Science Act to establish the new facility.

> *"We are excited to build a state-of-the-art advanced packaging facility in Indiana. We believe this project will lay the foundation for a new Silicon Heartland, a semiconductor ecosystem centered in the Midwest Triangle. This facility will create local, high-paying jobs and produce AI memory chips with unmatched capabilities, so that America can onshore more of its critical chip supply chain. We are grateful for the support of Govenor Holcomb and the state of Indiana, of President Chiang at Purdue University, and of the broader community involved, and we look forward to expanding our partnership in the long run."*
>
> **Kwak Noh-Jung,** Sk hynix CEO

PHOTO

Left to right:

Mung Chiang, *President, Purdue University*

Eric Holcomb, *Indiana Governor*

Kwak Noh-Jung, *President and CEO, SK hynix*

Woojin Choi, *Executive Vice President, SK hynix*

Arati Prabhakar, *Director, White House Office of Science and Technology Policy and Assistant to the President for Science and Technology*

Todd Young, *U.S. Senator*

Arun Venkataraman, *U.S. Department of Commerce Assistant Secretary*

Hyundong Cho, *Ambassador of the Republic of Korea to the United States*

David Rosenberg, *Indiana Secretary of Commerce*

Mitch Daniels, *Chairman, Purdue Research Foundation*

ASML – Purdue Partnering on Multiple Levels

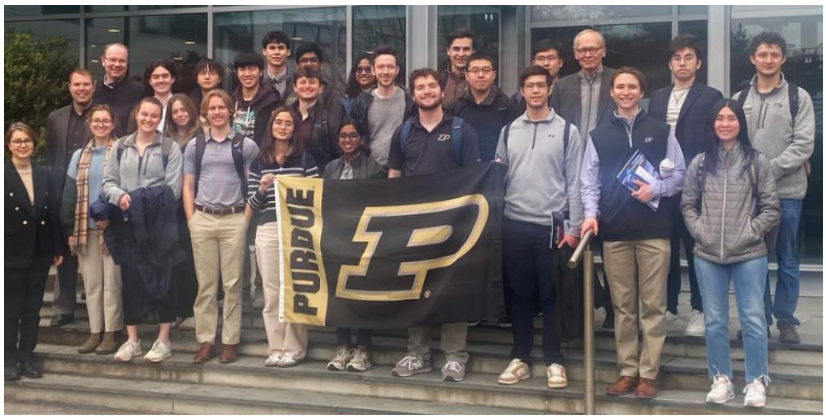
Purdue University is expanding its partnership with multinational tech company ASML, an innovation leader in semiconductor lithography, to include talent development, curriculum design, experiential learning, and R&D.

ASML is a founding member of the Purdue Semiconductor Degree Leadership Board, established in 2022. Dr. Anthony Yen (BSEE 1985), Vice President and Head of ASML's Technology Development Center, now serves as the Board's Co-Chair. Dr. Ronald Goossens, industry expert and longtime contributor to ASML, has been appointed as adjunct professor in the Elmore Family School of Electrical and Computer Engineering. He is working on developing a series of three one-credit semiconductor courses that will be launched in summer 2024:

"Introduction to Nanolithography" will provide a comprehensive introduction into lithography technology used in making semiconductor chips. "EUV Lithography" will cover lithography technology used in fabricating today's most advanced semiconductor devices. "Computational Lithography" will cover modeling and optimization of imaging on silicon wafers for a variety of design patterns, to result in the largest lithographic process window.

This year, ASML began working closely with Professor Weng Chew and the Consortium on Electromagnetics Technologies at Purdue to provide a new, math-physics modeling method for light scattering by lithography masks. This project aims to the develop new, more efficient modeling using computer simulation codes.

ASML engages hundreds of Purdue students through the "Changing the World with Chips – Introduction to Semiconductors" course with lectures by Dr. Michael Lercel, Senior Director of Strategic Marketing, regular participation in Purdue job fairs, and info sessions for graduates and undergraduates as part of the annual ASML Day at Purdue. In March 2024, ASML welcomed student groups from Purdue at its global headquarters in the Netherlands and at ASML Silicon Valley, its U.S. office in San Jose. Those visits gave students a solid understanding and first-hand experience of the equipment produced by the company. ASML is also a strong supporter of Purdue's unique quasi-internship program Summer Training, Awareness, and Readiness for Semiconductors (STARS). Several Purdue students are part of elite cohorts of interns who work at ASML sites in the U.S. or at company headquarters in Veldhoven, The Netherlands. Purdue and ASML hope this multifaceted collaboration will serve as a model for university corporate partnerships in the semiconductor industry. We are proud to have this partner as we take our next giant leap in semiconductors.



Purdue undergraduate students at the Eindhoven, Netherlands, global ASML headquarters, March 2024. At the same time, a similar Purdue student team was visiting the ASML San Jose location.

ASML Team conducting the EUV Challenge on the West Lafayette, Purdue Campus, March 2024.

Industry Partners

Design: AMD, Apple, Cadence, Graphcore, IBM, Intel, MediaTek, Nantero, NVIDIA, Reliable MicroSystems, Samsung, Silvaco, Synopsys, Qualcomm

Tooling: Applied Materials, ASM, ASML, Dassault Systémes, eFabless, Horiba, KLA, Lam, Teradyne, Tokyo Electron

Manufacturing: Amkor, Draper, Everspin, GlobalFoundries, IBM, Infineon, Intel, Marvell, Microchip Technologies, NHanced, Samsung, Seagate, SK hynix, SkyWater, Svagos, TSMC, Western Digital

Materials: Air Liquide, Air Products, Corning, Dow, Dupont, Eastman, Hemlock Semiconductors, Horiba, MacDermid Alpha, Molex

Customers: Amazon Web Services, Analog Devices, Apple, BAE Systems, Boeing, BorgWarner, Caterpillar, Cisco, Collins Aerospace, Cummins, Daimler, Deere & Co., Fiat Chrysler, Ford, General Dynamics, General Electric, General Motors, Google, Hewlett Packard Enterprise, Hitachi, Honeywell, Juniper Networks, L3Harris, LG Electronics, Lockheed Martin, Medtronic, Microsoft, Nokia, Northrop Grumman, One Network, Robert Bosch, Rolls-Royce, RTX, Saab, Siemens, SpaceX, Subaru, Tesla, Texas Instruments, Toyota, United Technologies, ZF Friedrichshafen AG (TRW)

How Industry Can Contribute to Developing the Semiconductors Workforce

Purdue University has already made significant investments in developing the next generation workforce for the semiconductors industry. We are looking forward to working with industry partners to take the initiative to the next level and encourage partners to contribute in many ways. Below are some examples of engagement—pick one option or all—Purdue is ready to work with you to create a customized program that fits your needs and maximizes student success. Contact Cristina Farmus cfarmus@purdue.edu to get more details.

In Kind

1. Commit to summer 2025 internships.
2. Commit to interviewing students with a GPA 3.2 and above.
3. Identify Purdue as a strategic partner university.
5. Provide speakers for undergraduate lecture series, high school outreach and college recruiting events.
6. Host faculty at your sites to better understand current industry needs.

Financial Support

1. Fund scholarships for students pursuing semiconductors degrees.
2. Support the Summer Training, Awareness, Readiness for Semiconductors (STARS) 2025 UG semiconductor program ($15K per student covers stipend, lodging, and program operating fees).
3. Sponsor VIP projects (e.g. tapeout fees).
6. Support new program/course development (e.g. MicroMasters).
7. Offer unrestricted support for semiconductor WFD.

Establish Permanent Presence at Purdue

Start as small or as large as you'd like, office space available immediately.

CEO Endorsements for the Purdue Semiconductor Degree Program

"The foundation of U.S. semiconductor leadership is America's talented technology workforce. It is critical we support and strengthen this workforce by creating, promoting, and investing in policies and programs that enable the training and retention of skilled semiconductor talent. I am thrilled Purdue University is taking a bold step in this mission with the creation of its new credentials and degrees focused on microelectronics and semiconductors at the undergraduate and graduate level. We strongly support these exciting and innovative initiatives."

John Neuffer | President and CEO, Semiconductor Industry Association (SIA)

"AI is the most impactful technology of our time. The automation of intelligence expands humanity's potential, enabling once-unimagined advances across science, industry and even the arts. Leadership in this era will require a new generation of engineers and computer scientists. It's exciting to see Purdue establish this program to prepare students for this challenge, enabling them to help shape fields from autonomous vehicles and robots to healthcare and climate science, and improve our world."

Jensen Huang | President and CEO, NVIDIA

"I am pleased to hear about the new graduate and undergraduate credentials and degrees on microelectronics and semiconductors being launched at Purdue University. These innovative and much-needed initiatives will play a key role in satisfying the voracious demand for skilled talent in the semiconductor industry. I am confident that graduates from this program will be in much demand at Lattice and other companies in our industry."

Jim Anderson | President and CEO, Lattice Semiconductor

"As one of the world's leading semiconductor manufacturers based in the U.S., GlobalFoundries strongly supports the efforts to grow U.S.-based semiconductor manufacturing. We recognize that to accomplish this goal, the shortage of semiconductor talent in the U.S. is a critical challenge the nation must address. I am pleased and encouraged to see Purdue University step up to this challenge by introducing a comprehensive set of degrees and credentials that will prepare students for exciting careers in semiconductors. We look forward to partnering with Purdue as these programs ramp up to support microelectronics across the U.S."

Thomas Caulfield | CEO and President, GlobalFoundries

"Today, semiconductors are more strategically and economically important to the world than ever and we need to significantly scale up the talent pipeline to support the future growth of our industry. Applied Materials is delighted to see Purdue University helping lead the charge to educate the tens of thousands of new engineers our industry needs through new degrees and credentials focused on microelectronics and semiconductors. We look forward to welcoming this next generation of innovators."

Gary Dickerson | President and CEO, Applied Materials, Inc.

"Every aspect of human existence is becoming digital, and everything digital runs on semiconductors. Increasing access to semiconductor and microelectronics education is essential for building a talented, diverse pipeline of future technologists. Intel plans to invest $100 million over the next decade to build a skilled semiconductor workforce in collaboration with universities, community colleges, and the NSF. I'm excited about Purdue's educational credentials focused on semiconductors and microelectronics, including the new interdisciplinary master's degree. With these timely and high-impact initiatives, Purdue is leading the way in bridging the skills gap and addressing the shortage of skilled human talent in the semiconductor industry."

Pat Gelsinger | CEO, Intel

CEO Endorsements for the Purdue Semiconductor Degree Program *(cont'd)*

"For three and a half decades, Synopsys has provided innovative design automation technology and products that catalyze the potential of semiconductor chips. Today, an exciting new era of microelectronics characterized by both scale and systemic complexity is beginning, and Purdue's new degrees and credentials will equip students with the practical skills needed in this new age. This initiative leads the way with the kind of comprehensive, innovative program that design automation and semiconductor companies, as well as the electronics ecosystem, critically need."

Aart de Geus | Chairman and CEO, Synopsys

"Semiconductors are the backbone of our digital society and global economy. Increasing investment in semiconductor education to train the next generation of technologists is vitally important for the long-term health and success of our industry. Purdue University's new graduate and undergraduate credentials and degree programs in semiconductors and microelectronics can serve as an incubator for the ideas and innovations of tomorrow. We strongly support this initiative and look forward to welcoming Purdue graduates to Marvell in the future."

Matt Murphy | President and CEO, Marvell

"It is essential for the United States to be a self-sufficient leader in semiconductor technology, which provides the foundation for the modern world and will lead to new innovations in critical industries. Purdue University's new credentials and degrees in microelectronics and semiconductors will help ensure that we have the large, skilled workforce that is needed to power the nation's semiconductor future."

Arvind Krishna | Chairman and CEO, IBM

"Semiconductor manufacturing requires a vast array of highly engineered and advanced materials and chemistries. CMC Materials and other leading materials companies look forward to supporting the expansion of semiconductors in the United States and globally. For the bold innovation in critical materials that is needed to advance technology and increase performance, a new generation of semiconductor engineers is critically needed. Purdue's new degrees and credentials will help students develop the depth and breadth needed for an exciting new era of technology that is just beginning. Kudos to Purdue for stepping up to address this key challenge for the U.S. semiconductor industry. Go Boilers!"

David Li | President and CEO, CMC Materials

"TSMC looks forward to being part of the resurgence of semiconductor manufacturing in the U.S. Success in this ambitious and critically important undertaking will require a much-expanded semiconductor talent with the knowledge and skills needed to innovate in a post-Moore's Law era. Purdue's innovative and comprehensive new suite of semiconductor degrees and credentials is exactly what is needed – at exactly the right time. We at TSMC look forward to working with Purdue to make this program a model for the nation."

Mark Liu, Chairman | TSMC

"Differentiated technologies that address a growing diversity of applications will characterize the next wave of electronics. This next wave will be driven by creative engineers with a broad understanding of microelectronics from materials, devices, and circuits to systems, packaging, and qualification. SEMI is delighted to partner with Purdue as part of the American Semiconductor Academy initiative, and I am pleased to see the university leading the way with the kind of comprehensive and innovative program that the semiconductor industry critically needs."

Ajit Manocha | President and CEO, SEMI

"Recent events have taught us all how critical chips are and how fragile supply chains can be, but a re-energized U.S. microelectronics landscape will require more than just building more fabs. As Moore's Law slows, new ways to advance the performance of electronics systems are needed, and this will require a new generation of bold and creative semiconductor engineers to pioneer equally as bold and creative semiconductor devices. I applaud Purdue in addressing this challenge with a comprehensive set of new semiconductor degrees and credentials that will help prepare a new generation of semiconductor engineers and address a critical need for Nantero and other companies."

Rob Snowberger | CEO, Nantero

"SkyWater sees tremendous value in partnering with Purdue University. They have tremendous faculty, researchers, and facilities around semiconductor creation. Their student body is developing into the workforce of the future, and with the new degree programs dedicated to semiconductors, those are just the graduates that SkyWater needs."

Thomas Sonderman | President and CEO, SkyWater

"We are entering an exciting new era of semiconductors with unprecedented demand driven by the need to execute artificial intelligence (AI) compute workloads. Graphcore is transforming the AI compute domain through innovative technologies that are going to be transformative across all industries and sectors with a real potential for positive societal impact from drug discovery and disaster recovery to decarbonization. Sustaining the rapid pace needed to have such an impact is going to require a big increase in the size of the semiconductor talent pool. I am excited to see Purdue leading the mission to educate the next generation of semiconductor workforce leaders by launching an innovative set of credentials and degrees. I expect this initiative to be a real difference-maker."

Nigel Toon | CEO, Graphcore

"Electronics is more and more often the differentiating factor in products, but the cost and complexity of design is exploding. As Efabless works to make custom chip design affordable and accessible to more companies, a critical challenge is the shortage of microelectronic talent. I applaud Purdue University for stepping up to this challenge. Purdue's new degrees and credentials meet prospective talent where they are with education and opportunity. This will help the next generation of students develop the knowledge, skills, and experience needed for an exciting new era of electronics."

Mike Wishart | CEO, Efabless

"We, at SRC, have sponsored more than 16,000 undergraduate and graduate research scholars and have a stated mission of building a diverse, inclusive, and highly trained workforce for tomorrow. Purdue's new credentials and degrees on microelectronics and semiconductors represent excellent and much-needed initiatives in semiconductor workforce development. We have a strong partnership with Purdue in the microelectronics revolution and look forward to further expanding this partnership to address the enormous possibilities for the industry and our country."

Todd R. Younkin | President and CEO, Semiconductor Research Corporation (SRC)

"My Purdue University degree laid the foundation for what continues to be a rewarding career. At RTX, we believe Purdue's Semiconductor Degrees Program will provide students interested in joining the microelectronics workforce with the valuable skills and experiences they'll need to achieve their own career goals, while helping strengthen the U.S. economy and national security. Semiconductors are a critical component that enables ground-breaking technology across the aerospace and defense industries. After completion, I can envision program graduates joining the thousand-plus Purdue alums who are already helping RTX create a safer, more connected world."

Gregory Hayes | Chairman and CEO, RTX

Purdue Semiconductor Degree Leadership Board

Purdue has launched the Semiconductor Degree Leadership Board (SDLB), an elite group of executives from leading semiconductor companies that provide visionary input into the Purdue Semiconductor Degrees Program and other workforce development programs designed and implemented by Purdue. Deirdre Hanford, former co-chair of Purdue University's Semiconductor Degrees Leadership Board, was appointed as CEO and trustee of the National Center for the Advancement of Semiconductor Technology (Natcast).

We are proud to list the following members:

NAME	TITLE	COMPANY
Keyvan Esfarjani	*SDLB Co-Chair* | Executive Vice President, Chief Global Operations Officer and General Manager of Manufacturing, Supply Chain and Operations	Intel
Anthony (Tony) Yen	*SDLB Co-Chair* | Vice President and Head of Technology Development Center	ASML
Gregg Bartlett	Chief Technology Officer	GlobalFoundries
Juan de Bedout	Senior Vice President of Aerospace Technology	RTX
Rick Burns	President, Semiconductor Test Division	Teradyne
William Chappell	Chief Technology Officer Strategic Missions and Technology (SMT) Division	Microsoft
Todd Citron	Chief Technology Officer	Boeing
Debra Delise	Vice President of Security Products and Technology	Analog Devices
Brian Dunlap	Vice President 300mm Fab Operations	Texas Instruments
Sudhir Gopalswamy	Senior Vice President and General Manager of the Advanced Solutions Group (ASG)	onsemi
Richard Gottscho	Executive Vice President	LAM Research
Brian Harrison	President	TSMC Arizona
Raghib Hussain	President of Products and Technologies	Marvell Technologies
Mohammed Kassem	CoFounder and Chief Technology Officer	Efabless
Mukesh Khare	General Manager of IBM and Vice President of Hybrid Cloud	IBM
Randal King	Vice President of Research and Development/Technology	Dupont Electronics and Industrial
Soo Yong Lim	Head of Pathfinding and Strategy, AI Infra and Head of Business Enabling Director Group, AI TF	SK hynix
Matt Massengill	Chairman of the Board and Former Chief Executive Officer	Western Digital
David McCann	Senior Vice President, Chief of Staff of Business Unit	Amkor Technology
Om Nalamasu	Senior Vice President and Chief Technology Officer	Applied Materials
John Neuffer	President and Chief Executive Officer	Semiconductor Industry Association
Alexander Oscilowski	President	Tokyo Electron Technology Center America
Mark Papermaster	Executive Vice President and Chief Technology Officer of Technology and Engineering	AMD

NAME	TITLE	COMPANY
Adam Peters	Chief Executive Officer, North America	Air Liquide Group
Nirmal Ramaswamy	Vice President of Advanced DRAM and Emerging Memory	Micron Technology
Thomas Rueckes	Chief Technology Officer and CoFounder	Nantero
Charlie Schadewitz	Vice President, North American Field Operations at Cadence Design Systems	Cadence
Stéphane Sireau	Vice-President, High-Tech Industry	Dassault Systémes
Thomas Sonderman	Chief Executive Officer	SkyWater
Ian Steff	President and Chief Executive Officer	mySilicon Compass, LLC
Edward Tiedemann	Senior Vice President	Qualcomm
Samuel Valenti	Vice President, Engineering and Technology	Space & Airborne Systems/ L3Harris Technologies
Ronnie Vasishta	Senior Vice President	NVIDIA
Brandon Wang	Vice President, Office of the CEO	Synopsys
Bruce Weyer	Vice President, FPGA Business Unit	Microchip
Patrick Wilson	Vice President, Government Relations	MediaTek
Philip Wong	Willard R. and Inez Kerr Bell Professor, ECE	Stanford University
Jie Xue	Vice President, Technology and Quality	Cisco Systems

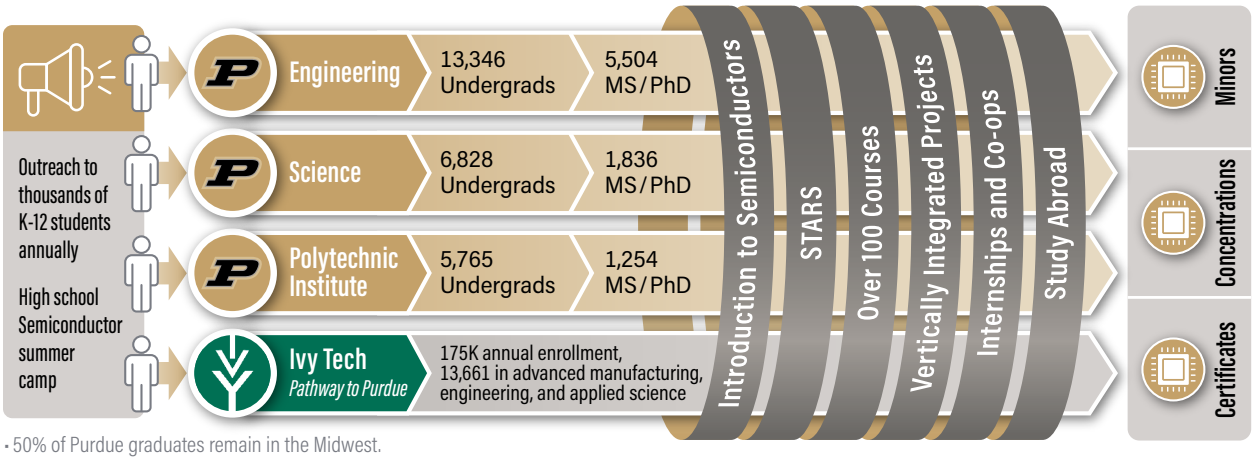
Semiconductor Degree Leadership Board with faculty and students at the Birck Nanotechnology Center for the Fall 2023 annual meeting.

Former SDLB co-chair Deirdre Hanford with Secretary of Commerce, Gina Raimondo at the signing event at the White House officially establishing the National Semiconductor Technology Center in February 2024.

Purdue Semiconductor Degree Program

Purdue's reputation as an R&D trailblazer is matched by its leadership in workforce development programs for semiconductors. Several programs described below attest to a strong University culture, a tradition of innovation in workforce development, and an array of recent successes related to microelectronics training at scale.

Purdue Semiconductor Pipeline → *Fall 2024 Enrollment Exceeded 34K STEM Student*



- 50% of Purdue graduates remain in the Midwest.
- Purdue conferred **7,561 BS, MS, and PhD** degrees to Engineering, Science, and Polytechnic Institute students in AY 2023-24.

TYPE OF DEGREE OR CREDENTIAL	RESIDENTIAL	ONLINE
Interdisplinary, 6-in-1 MS Degree	✓	✓
Graduate Concentration (MS and PhD)	✓	✓
Stackable Certificates	✓	✓
Undergraduate Concentration and Minor	✓	
Introduction to Semiconductors Freshman Course	✓	✓

Purdue is the first U.S. university to launch a comprehensive set of minors and concentrations for undergraduates, Masters programs, and certificates, residential and online, dedicated to semiconductors along its entire supply chain to address the nation's critical need for microelectronics engineers.

Internships, Co-Ops, and Learning While Working

Purdue runs one of the largest and best undergraduate industry internship and co-op programs in the nation. Besides the inaugural semiconductor suite of degrees, Purdue has also created a Learning While Working program, enabling students to work towards their degrees while working full time. A good number of companies are subscribing to this model, running in parallel with internship and co-op programs. **For more information, visit:** https://www.opp.purdue.edu/

Partnerships

Recognizing the need to contribute to the entire range of microelectronics workers, Purdue is partnering with Ivy Tech Community College to develop several programs aimed to increase the number of technicians and also to strengthen the pipeline for four-year degrees. Ivy Tech has more than 40 locations across Indiana and teaches classes in more than 75 communities serving nearly 100,000 students annually. Ivy Tech is the largest public postsecondary institution in Indiana and the largest singly-accredited statewide community college system in the country. Additional partnerships are explored with academic partners, such as Rose Hulman Institute of Technology.

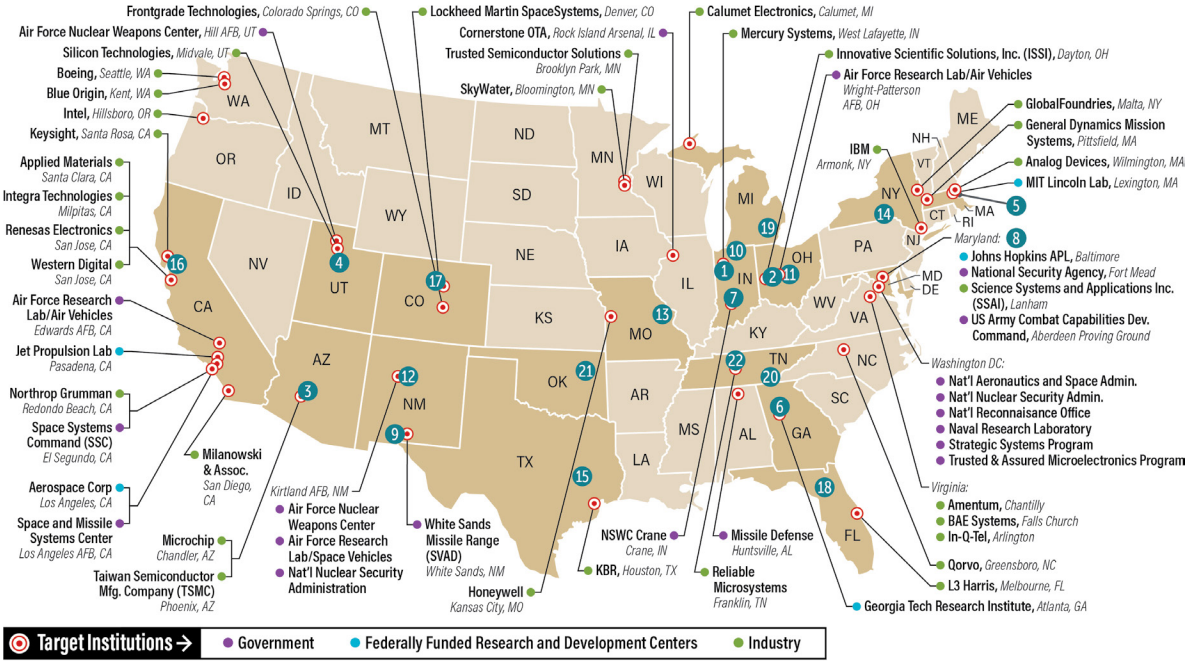
SCALE DoD Microelectronics WFD Center

Purdue University is leading a five-year, DoD-sponsored national initiative aimed at addressing the urgent need to develop a highly skilled U.S. microelectronics workforce to bolster national security. Comprising of 19 partner universities across the country, Scalable Asymmetric Life Cycle Engagement (SCALE) is a $65M—with a funding ceiling up to $99M—public-private-academic partnership formed to advance the technical capabilities of the domestic microelectronics workforce, and to motivate talented STEM undergraduate and graduate students to pursue federal government careers in the semiconductor field.

SCALE is being managed in partnership with the Naval Surface Warfare Center Crane Division as a nationally coordinated network of government, industry, and university partners, with regional execution. Faculty from across Purdue's College of Engineering are collaborating with experts from 19 other universities, the DoD, NASA, the Department of Energy NNSA labs, and the defense industry to create a microelectronics workforce focused on national security needs.

The workforce development program provides microelectronics modules, mentoring, public- and private-sector internship matching, and targeted research projects for college students interested in these microelectronics specialty areas:

- Radiation hardening
- Heterogeneous integration/advanced packaging
- System-on-chip electronics
- Embedded systems security/trusted artificial intelligence (AI)
- Radio frequency Optical electronics



Partners

↓ (Institution Topic Areas)

ESS/TAI .. Embedded Systems Security/Trusted AI
HIAP ..... Heterogeneous Integration/Advanced Packaging
RH ..... Radiation Hardened,
RF/OE .... Radio Frequency/Opto Electronics
SoC ..... System on Chip

1. **Purdue University** *West Lafayette, IN* (RH, HIAP, SC)
2. **Air Force Institute of Technology** *Wright-Patterson AFB, OH* (RH)
3. **Arizona State University** *Tempe, AZ* (RH, HIAP)
4. **Brigham Young University** *Provo, UT* (RH)
5. **Draper Laboratory** *Campridge, MA* (RH)
6. **Georgia Institute of Technology** *Atlanta, GA* (RH, HIAP, SoC)
7. **Indiana University** *Bloomington, IN* (ESS, SoC)
8. **Morgan State University** *Baltimore, MD* (SoC)
9. **New Mexico State University** *Las Cruces, NM* (RH)
10. **Notre Dame University** *South Bend, IN* (ESS/TAI)
11. **Ohio State University** *Columbus, OH* (SoC)
12. **Sandia National Laboratory** *Albuquerque, NM* (RH)
13. **St. Louis University** St. Louis, MO (RH)
14. **SUNY Binghamton** Binghamton, NY (HIAP)
15. **Texas A&M University** Commerce, TX (CSME)
16. **University of California** Berkeley, CA (SoC)
17. **University of Colorado Boulder** Boulder, CO (RF/OE)
18. **University of Florida** Gainesville, FL (CSME)
19. **University of Michigan** Ann Arbor, MI (SoC)
20. **University of Tennessee at Chattanooga** Chattanooga, TN (RH)
21. **University of Tulsa** Tulsa, OK (ESS/TAI)
22. **Vanderbilt University** Nashville, TN (RH)

SCALE Faculty include: Peter Bermel (Principal Investigator), Kerrie Douglas (Program Director), Tom McKinley (Managing Director), Ashraf Alam, Joerg Appenzeller, Shubhra Bansal, Nikhilesh Chawla, Allen Garner, Selcen Guzey, Carol Handwerker, Eric Holloway, Morgan Hynes, Mark Johnson, David Johnson, Jenn Linvill, Amy Marconnet, Saeed Mohammadi, Tamara Moore, Anand Raghunathan, Vijay Raghunathan, Kaushik Roy, Shreyas Sen, Alejandro Strachan, Ganesh Subbarayan, and Justin Weibelw

For more information, visit: https://www.purdue.edu/discoverypark/scale/index.php

Purdue Summer Training, Awareness, and Readiness for Semiconductors (STARS)

Program Description: Purdue University has developed STARS, an intensive eight-week semiconductor training program offered annually on the Purdue campus. This program helps students develop deep-tech skills. The STARS 2025 program will have several tracks focused on chip design, semiconductor manufacturing, advanced packaging and heterogeneous integration, and supply chain optimization. Students will participate in hands-on experiential learning activities in the **Scifres Nanotechnology Cleanroom** and other labs at Purdue from May 29 to July 11, 2025.

Target Students: STARS is designed to be the academic equivalent of a summer internship for Purdue rising sophomores in engineering and science disciplines, and a few participants from Ivy Tech Community College. After completion of STARS, students are encouraged to pursue other relevant courses at Purdue towards earning a semiconductor concentration or certificate. Preference will be given to students who have participated in the **Changing the World with Chips—Introduction to Semiconductors** course offered in Fall 2024 and Spring 2025. (https://engineering.purdue.edu/semiconductors).

Program Cost: The full cost of the program per participant is $15,000, ($10,000 to cover a competitive student stipend and $5,000 program management costs such as materials, design kits, access to the cleanroom, and instructors.)

Industry Request for Support: We aim to train 100 students in summer 2025 and seek industry support at $15,000 per student to reach our goal. If you'd like to sponsor STARS, please contact Matthew Merzdorf, Director, Office of Industry Partnerships, at mrmerzdorf@purdueforlife.edu or 765-427-5775. Purdue will provide invoices if needed. We are confident the Purdue programs will be foundational to address our national need for more semiconductor professionals in the coming decades.

To follow our progress on STARS, visit our **For Students** page at https://engineering.purdue.edu/semiconductors.

Purdue students on the first day of the STARS 2023 program.

Summer 2024 STARS Highlights

During Summer 2024, Purdue engaged 98 students in the Summer Training, Awareness, and Readiness for Semiconductors (STARS) Program, either as students or as teaching assistants.

> *"Without this program, I don't think I would have ever really thought to go into this industry, even though it is becoming so big."*
>
> **Raygan Bingham,**
> Mechanical Engineering Sophomore

Total Students: 98

- 24 women
- 11 underrepresented minorities
- 20 international students
- 88 Purdue University

Universities Represented

- 7 Ivy Tech Community College
- 1 Carnegie Mellon University
- 1 Iowa State University
- 1 University of Puerto Rico, Mayaguez Campus

Majors Include

- 52 Electrical Engineering
- 14 First-Year Engineering
- 9 Mechanical Engineering
- 6 Purdue Polytechnic Institute
- 5 Computer Science
- 3 Materials Engineering
- 1 Chemical Engineering
- 1 Aeronautics and Astronautics

Industry Benefits

STARS is a one-of-a-kind program that will attract students early towards a semiconductor career. Purdue provides quality, intensive training for students who may not yet have sufficient skills or knowledge to find an internship in semiconductors and might steer to other industries with lower barriers to entry. Companies that sponsor STARS will have input in the activities planned and privileged access to the student cohort, such as access to resumes and mentorship opportunities. $15,000 per student is a good investment for a summer intern, with no overhead or liability, and minimum time investment from the company to mentor them virtually during the summer. Students who completed STARS will be prepared for Co-Op opportunities or internships as early as fall 2024. Companies are encouraged to interview the students after they complete the STARS internship on campus, but they do not have an obligation to hire these students.

Thank You to our 2024 Sponsors!

AMD, Amkor Technology, ASML, cadence, efabless.com, GlobalFoundries, intel, L3HARRIS, Lam Research, Lilly Endowment, MARVELL, MEDIATEK, Microchip, SK hynix, skywater, Synopsys, TEL Tokyo Electron, Texas Instruments, tsmc, Western Digital

Photos: *2024 STARS Manufacturing/ Packaging and Design students at their end of the summer graduation.*

(Photos: Vincent Walter)

Student testimonies are available at:
https://stories.purdue.edu/seeing-stars-purdue-trains-next-generation-of-semiconductor-engineers/

Purdue–Ivy Tech Chips Program (PITCH)

For the second year in a row, 60 students from six counties and 12 different high schools in and around Tippecanoe County and the Greater Lafayette area have completed a two-week program that could give them a leg up in the rising semiconductor industry. The students were recognized for this achievement on June 14th, 2024 during a graduation ceremony inside the Hall for Discovery and Learning Research (DPD).

The event was the culmination of a partnership between Purdue University and Ivy Tech Community College to develop a talent pipeline of students and increase technician and engineer training to support the region's expected workforce demand for advanced semiconductor manufacturing. That demand is largely due to the planned construction of SK hynix's $4 billion investment to build an advanced packaging fabrication and R&D facility for AI products in the Purdue Research Park. The company plans to bring at least 800 new jobs to West Lafayette.

In addition to building a wearable sensor and learning how to program a robot, the group of rising juniors and seniors, who split their time between Purdue and Ivy Tech, gained exposure to printed electronics and solar cells, designed and fabricated their own printed circuit boards (PCBs) to measure the state-of-charge of a battery, and used semiconductors to solder electronic components onto their PCBs. Ultimately, students worked together in small teams in a three-day workshop to create their own custom projects out of paper electronics, which include a robo-spotter to automate safety in weightlifting, for personalized data dashboards, and an electronic safe. Also included in Ivy Tech's portion of the program was an overview of the soft skills required to be successful in the semiconductor industry. Participants attended a workshop to develop elevator speeches, then delivered them to peers and instructors.

Organizers are planning for summer 2025, when the program is expected to continue with even more students.

Semiconductor Student Alliance—Purdue Chapter

The Semiconductor Student Alliance—Purdue Chapter (SSA) is a newly founded student organization allowing students to become a part of the Semiconductors@Purdue initiative and achieve their highest potential with the many opportunities within the semiconductor field. The Semiconductor Student Alliance—Purdue Chapter plans to bolster workforce development and foster student engagement by advertising semiconductor programs, establishing industry relationships, and communicating unique research opportunities for Purdue University students.

The first step taken to achieve these goals was with SSA's first callout joined by Intel on February 12th, 2024. Intel provided information on what the next generation of the semiconductor workforce will entail and how each student can become an essential part of it. After each callout, the organization will create resources for members to get involved with and be informed of the sponsoring party's opportunities. In addition to callouts, SSA plans to develop recruiting events to reinforce the pipeline of Purdue University students and semiconductor industry leaders. The chapter will be hosting a conference for students from Purdue and universities in surrounding states in November 2024.

If you are a company representative interested in co-sponsoring an event with SSA, please reach out to daygun@purdue.edu so the SSA team can make it happen.

Joseph Lopez (center) with Purdue President Mung Chiang and Chief Semiconductor Officer Mark Lundstrom (left).

2024 SSA Board Members.
Left to right: Dilay Aygun, Miguel, Isrrael Teran, Andrew Schlabach, Thomas Munson, Carl Hahn, Ethan Baird (not pictured: Joseph Lopez)

(Photo: Hyun Kim)

Chipshub—Global Online Workforce Development

Purdue Engineering Online

nanoHUB is a vibrant and inclusive community with broad usage at U.S. institutions of higher learning—44% of all technical institutions and 77% of all technical minority serving institutions have used nanoHUB tools. Each year, over 1 million global visitors access state of the art educational content including full length courses, focused short courses, free textbooks, and powerful simulation engines and userfriendly apps, all in the cloud.

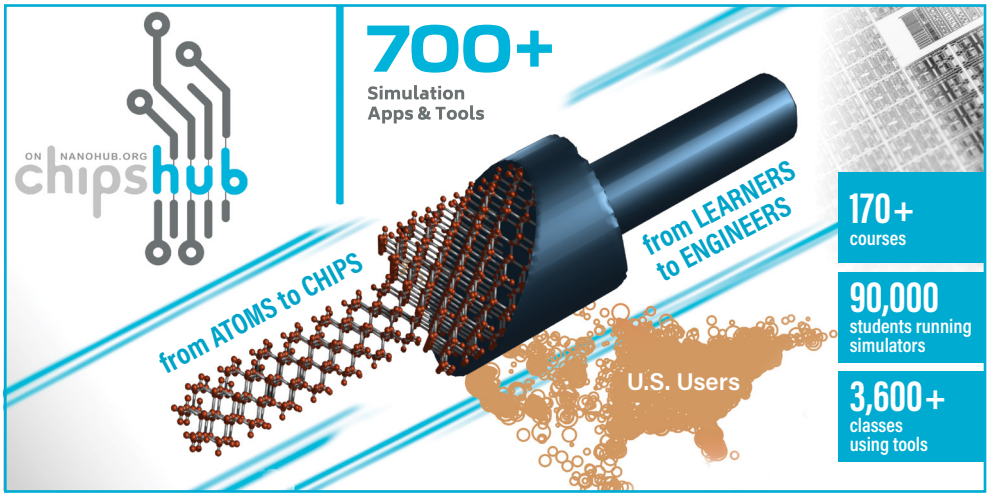
nanoHUB supports semiconductor workforce development at scale, providing industry-strength engineering tools, opensource and research-based tools that do not require students or instructors to download, install, license, support, or maintain the software. Instead, nanoHUB's apps and tools are accessible through any web browser and run on nanoHUB's computing cloud. Modeling, simulation, and data are available to users as both stand-alone tools and part of structured teaching and learning curricula.

nanoHUB hosts over 700 apps and tools that have been used by over 180,000 simulation users. 90,000+ of these were students in 3,600+ classes. Nearly 7,000 other content items provide educational scaffolding around these tools. A subset of nanoHUB's resources is curated in a special group page for semiconductor workforce development. https://nanohub.org/groups/semiconductoreducation

From nanoHUB.org to chipshub.org—From Atoms to Chips

nanoHUB began in 1995 as one of the first web portals to provide access to scientific simulation tools via web forms. Even before the Apple iPhone, nanoHUB was creating user-friendly, easy-to-use Apps and created the first scientific end-to-end cloud before the "cloud" became a thing. Notably, in 2017 the Web of Science began listing nanoHUB Apps and Tools as a new type of digital publication. nanoHUB has demonstrated that it can overcome the barriers of entry to using computational simulation tools and project collaboration that were posed by complex software installation, software licensing, and computation hardware provisioning.

Chipshub builds on nanoHUB's demonstrated competencies in delivering both open-source and commercial software in a simple-to-use cloud environment, provisioning needed educationally scaffolded materials, and building a community that rapidly embraces workforce development at scale. nanoHUB already hosts several commercial tools from SILVACO, ThermoCalc, and MATLAB. We are installing Cadence tools right now and are in license discussions with both Synopsys and Siemens. In addition to design tools, the Chipshub infrastructure will enable chip manufacturing to be performed, seamlessly, with nanoHUB's partners. "From lab to fab": Using Chipshub, students will be able to architect, design, optimize, and test chips in a single platform without any software installation, and faculty will be empowered to adopt newly available educational resources.



We envision Chipshub will impact over 220,000 U.S. engineering students and specifically over 49,000 designers over 5 years.

Semiconductor Facilities

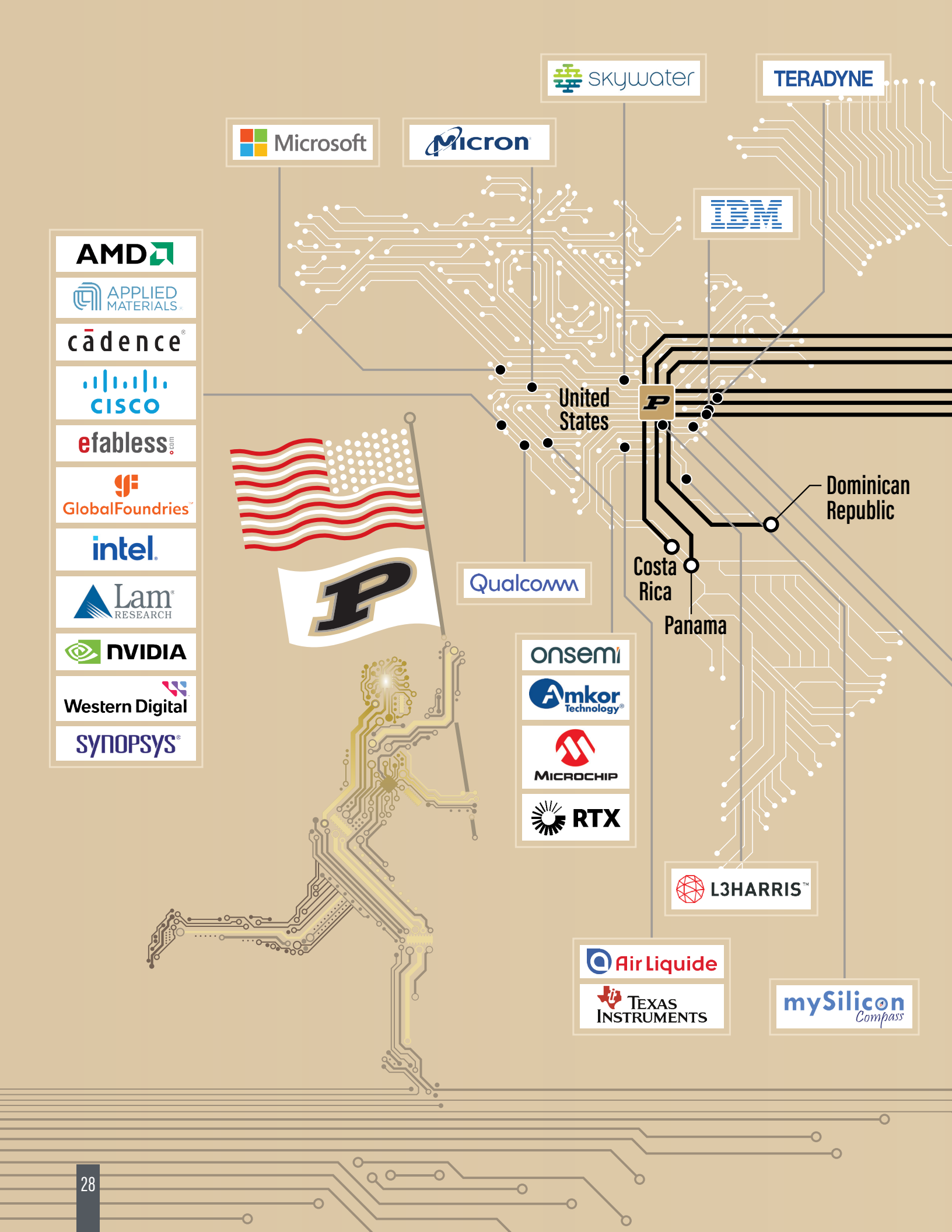
Purdue Investing $100 million in Semiconductor Facilities

For a virtual tour of Birck Nanotechnology Center, go to:
https://www.purdue.edu/discoverypark/birck/

Purdue University has announced $100 million of semiconductor facility updates with phase one of $49 million being approved by the Purdue Board of Trustees in April of 2023, for capital project and equipment procurement to upgrade the 18-year-old national treasure Birck Nanotechnology Center. The $49 million project will increase cleanroom space, add fabrication and characterization equipment and capabilities, and enhance the facility's capacity to support the lab-to-lab transition for CHIPS Act initiatives. This enhanced state-of-the-art facility will also support Purdue's broader, longterm research goals. The goals of the CHIPS and Science Act are to advance microelectronics and advanced packaging research and foster collaborations with industry partners. This project will enable Purdue to support this mission by providing Birck researchers with the resources they need to accelerate innovation, work efficiently with industry collaborators, and achieve the goals of CHIPS and Science Act through development of new technologies that can revolutionize the semiconductor industry. Purdue is committed to driving innovation and economic development, and this project underscores Purdue's commitment to providing critical resources to help our researchers become even more impactful. By supporting industry collaborations and the lab-to-fab transition, the Birck Nanotechnology Center is playing a critical role in helping to bring cutting-edge technologies to manufacturing. Construction on the project is expected to begin in the Fall of 2023, with completion targeted for Fall of 2024.

About the Birck Nanotechnology Center

The Birck Nanotechnology Center at Purdue University is a multidisciplinary research facility that includes professionally staffed 25,000 square foot. Scifres Nanofabrication Laboratory cleanroom and its state-of-the-art suite of tools. Together with specialized characterization labs throughout the Birck facility, this creates an environment for the research community to design, fabricate and characterize materials and devices at the nanoscale and integrate them at the advanced system and packaging level. Birck enables collaboration among faculty, researchers, and staff engineers, and facilitates partnerships with other academic institutions, industry, and government. It serves as a platform for public and private partnerships, bringing together diverse expertise and resources to address pressing challenges in the field of nanotechnology.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IBM
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APPLIED MATERIALS
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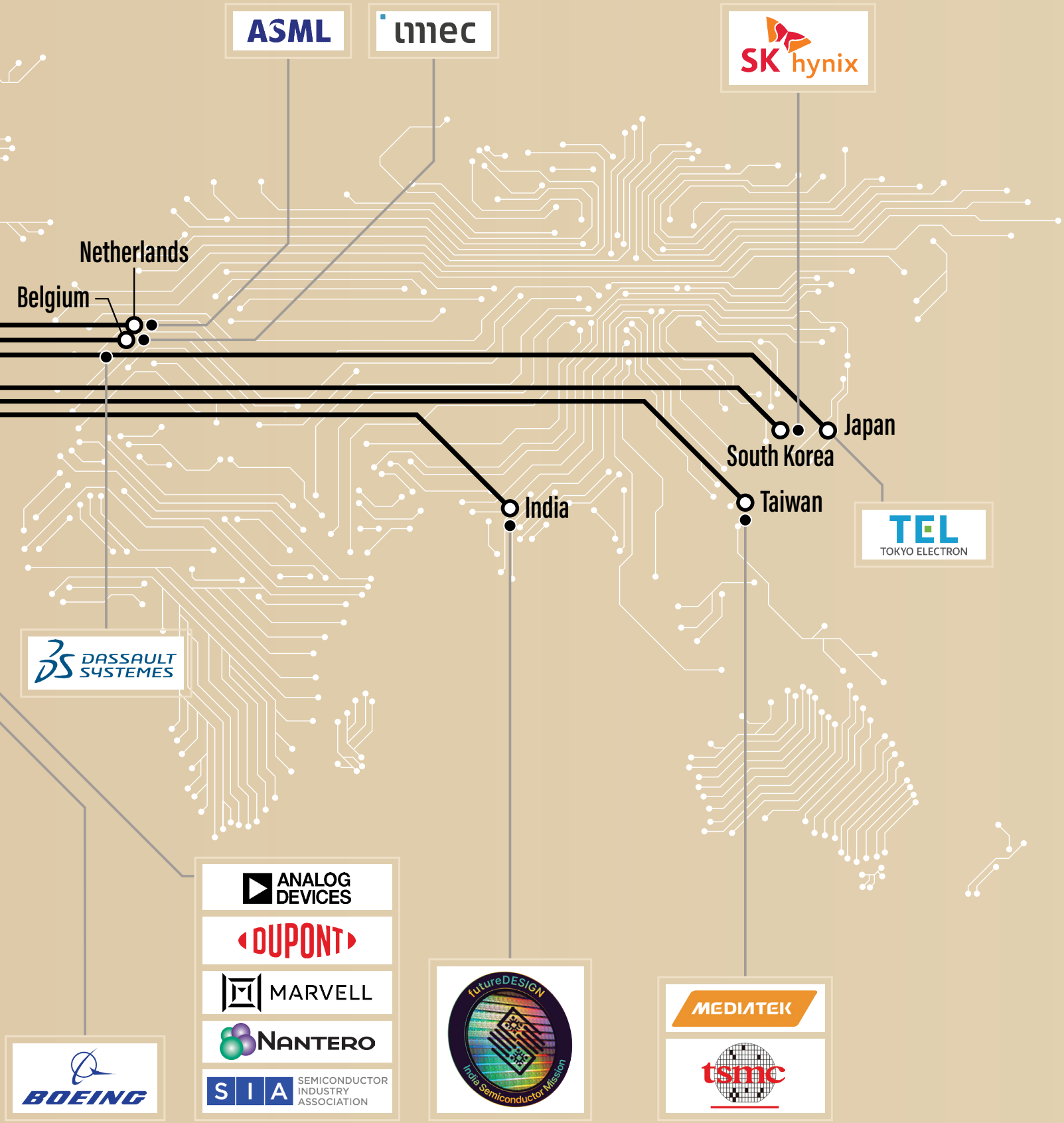


Purdue International Partnerships on Semiconductors

Mediatek Opens New IC Design Center at Purdue University

JUNE 28, 2022

On June 28, 2022, Purdue University announced a partnership with MediaTek Inc., a leading global fabless chipmaker, to open the company's first semiconductor chip design center in the Midwest, to be housed on Purdue's campus. MediaTek and Purdue also will partner on new chip design engineering degree programs, research on artificial intelligence, and communications chip design. This collaboration is still in the works.

"This means students and faculty at Purdue will have the opportunity to interact with world class chip design talent right across the street," said Dr. Mung Chiang, President of Purdue University. The Purdue team worked with the Indiana Economic Development Corporation to fully leverage Purdue's role as one of the top STEM universities to attract this new semiconductor investment.

"We believe strongly that being in Indiana means we'll have access to some of the best engineering talent in the world," said Dr. Kou-Hung Lawrence Loh, Corporate Senior Vice President of MediaTek Inc. and President of MediaTek USA, Inc. "Not just at Purdue, but West Lafayette is only four hours away from nearly a dozen of the top engineering schools in the country. In the post pandemic world, top candidates tell us they want to be closer to home, near family and they want to have a real house and great schools. Indiana offers all that and more."

The Purdue partnership represents a new U.S. growth model for MediaTek USA—outside the traditional centers of gravity for chip design.

Among those who participated in the announcement were Kou-Hung Lawrence Loh, Corporate Senior Vice President of MediaTek Inc. and President of MediaTek USA (second from left), Eric J. Holcomb, Governor of the State of Indiana (third from left), Brad Chambers, Indiana Secretary of Commerce (fourth from left), and Mung Chiang, President of Purdue University (far right).

European Technology Leader imec Opens Innovation Hub at Purdue

DECEMBER 8, 2023

On December 8th, 2023, Purdue University and Belgium-based technological innovation organization imec celebrated the grand opening of a research and development hub at the Convergence Center for Innovation and Collaboration at Purdue's campus. The presence of imec at Purdue will help facilitate groundbreaking advancements in semiconductor technologies. To mark the occasion, Purdue President Mung Chiang was joined by Luc Van den hove, President, and CEO of imec, and Jan Jambon, Minister-President of Flanders, the Flemish region of Belgium, following their visit with the Indiana Economic Development Corporation (IEDC) and Govenor Eric Holcomb in Indianapolis. The Purdue location represents imec's first Midwest research office, adding to its offices in California and Florida. With imec and IEDC's investment, researchers from the global R&D technology company will work side by side with faculty and students at the Birck Nanotechnology Center, located in Discovery Park District at Purdue. Similarly, students and faculty will have an opportunity to work in Belgium.

> *"Purdue is established as a leading university in semiconductors through successes such as the Department of Defense Microelectronic Commons Hub, SCALE workforce consortium, U.S.-Japan semiconductor alliance, U.S.-India semiconductor partnership and more. This partnership with imec, the crown jewel of chips innovation in Europe, will flourish as a strategically pivotal moment in the growing ecosystem of semiconductors in the heart of the Silicon Heartland. It also builds a bridge between our university and universities and companies in Flanders, in Belgium, and in Europe."*
>
> **Mung Chiang,** Purdue University President

(Photo: Purdue University)

Imec President and CEO Luc Van den hove, Purdue President Mung Chiang, and Flemish Minister-President Jan Jambon celebrate the grand opening of a research and development hub for semiconductor technologies at Purdue's Convergence Center.

U.S.–Japan University Partnership for Workforce Advancement and R&D in Semiconductors (UPWARDS) for the Future—*Meeting at Purdue*

OCTOBER 18, 2023

The CHIPS and Science Act, signed into law on August 9, 2022, envisions new opportunities in accelerating progress in key technology areas, building the STEM workforce of tomorrow, and fostering partnerships with the private sector to enable this progress. It offers a unique and historic opportunity to expand the nation's capacity for semiconductor production as well as to prepare the U.S. workforce for jobs in advanced manufacturing and engineering. Recognizing that a skilled and diverse pipeline of workers is vital to building a sustainable semiconductor industry, collaboration between government, academia, and the semiconductor industry is needed to ensure that education and research training programs are aligned with industry needs and that students are well-prepared to fill critical, in-demand roles. The U.S.-Japan UPWARDS for the Future represents a collaboration between six U.S. universities and five Japanese universities, working with industry partners to provide advanced training and research opportunities to students, faculty, and professionals in an effort to address the demand for a highly trained microelectronics and semiconductor workforce and, as a result, build global and domestic capacity in the semiconductor field. Activities to achieve such goals include targeted student exchange programs, professional certification opportunities, curriculum development, visiting faculty/researcher programs, and focused research projects leveraging the resources and expertise from each partner. Through a shared commitment to training and research, partners will complement and scale current efforts to broaden and support the semiconductor workforce pipeline.

Purdue University hosted the inaugural meeting of the UPWARDS Network for workforce advancement and research and development in semiconductors. As announced at the G7 meeting in May 2023 in Japan, Micron Technology and Tokyo Electron US, as founding industry partners, the U.S. National Science Foundation (NSF) and universities together will invest over $60 million for the five-year project.

Purdue and India Semiconductor Alliance

MAY 9, 2023

On May 9th, 2023, Purdue President Mung Chiang signed an agreement establishing itself as a key collaborator with India and the India Semiconductor Mission (ISM) in skilled workforce development and joint research and innovation in the burgeoning fields of semiconductors and microelectronics. Purdue signed the agreement with the leadership of the India Semiconductor Mission in the presence of Honorable Minister Ashwini Vaishnaw, who is in charge of Railways, Communications, Electronics and Information Technology in India and also oversees the country's semiconductors program. With the agreement, Purdue will focus on:

1. Creating cutting-edge online and hybrid academic programs for specialized training in areas including chip design and fabrication, advanced packaging, semiconductor materials, and embedded system design that can be made available to Indian students as ISM-endorsed training programs, both as noncredit offerings and through integration into the curricula of Indian educational institutions.
2. Exploring the creation of dual-degree programs in semiconductors and microelectronics with Indian educational institutions.
3. Joint research and development programs aimed at designing, manufacturing, and commercializing semiconductor chips.
4. Driving technological advancement and strengthening bilateral relations between the U.S. and India by facilitating collaborations with Indian educational institutions and companies, to obtain joint funding opportunities in the areas of semiconductor research and chip design, manufacturing, and commercialization.

Purdue's Memoranda of Understanding (MOU) with India and ISM is for five years, with the opportunity to renew. This collaboration aligns with ISM's mission of driving India's strategies for developing a comprehensive semiconductors and display ecosystem. The agreement falls under the Semiconductor Supply Chain Innovation Partnership, signed by the U.S. and India on March 10th, 2023. It is also aligned with the U.S. and India initiative on Critical and Emerging Technology (iCET) partnership launched by the National Security Advisors of the U.S. and India in January 2023, collaboration in emerging and critical technologies, including semiconductors, artificial intelligence and quantum computing.

Left to right:

Dr. T.V. Nagendra Prasad, *Consul General of the Indian Consulate in San Francisco*

Hon. Ashwini Vaishnaw, *India's Union Minister for Railways, Communications, Electronics and IT*

Prof. Mung Chiang, *President, Purdue University*

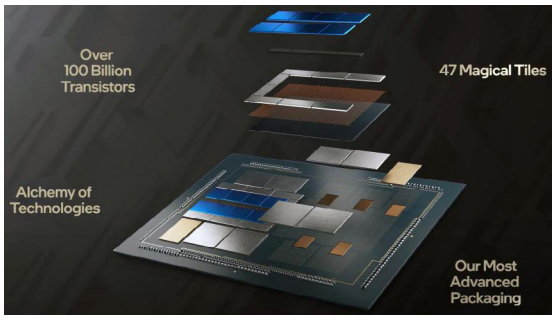
Prof. Vijay Raghumathan, *Director of Semiconductor Education, Purdue University*

(Photo: Purdue University)

Research Centers

C-BRIC

The Center for Brain-inspired Computing (C-BRIC) is funded by SRC and DARPA under the JUMP center program. Led by Professors Kaushik Roy (Director) and Anand Raghunathan (Associate Director), C-BRIC has a mission to deliver key advances in cognitive computing that will enable a new generation of autonomous intelligent systems such as self-flying drones and interactive personal robots. C-BRIC is led by Purdue and includes researchers from 11 universities working on neuro-inspired algorithms and theory, neuromorphic computing fabrics, and distributed intelligence. C-BRIC brings together experts from machine learning, computational neuroscience, theoretical computer science, integrated circuits and systems, distributed computing, robotics, and autonomous systems to pursue improvements in cognitive systems that are difficult for these communities to achieve independently.



CHIRP

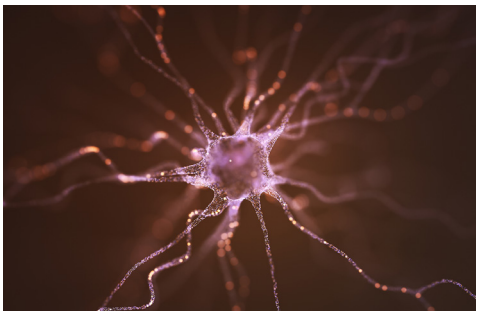
The Center for Heterogeneous Integration Research on Packaging (CHIRP) is co-directed by Ganesh Subbarayan of Purdue and Bahgat Sammakia of SUNY Binghamton. CHIRP's mission is to enable the building of future Systems-in-Package through Heterogeneous Integration. The areas of CHIRP research focus include design enablement, global interconnects, power delivery, thermal management, modeling, metrology, and reliability that together optimally address the power, performance, area, and cost metrics of systems. CHIRP also works to educate engineers who can design and build heterogeneously integrated systems. The center was established in 2019 with support from ARM, Intel, IBM, MediaTek, NXP, Samsung, and Texas Instruments, and has since funded over $6M in projects. CHIRP engages nearly 20 investigators from Purdue and SUNY Binghamton.

NEW LIMITS

The NEW Materials for LogIc, Memory and InTerconnectS (NEW LIMITS) center is directed by Professor Zhihong Chen. The center's vertically integrated mission is to develop synthesis, integration, and evaluation schemes for new materials that will be used in unique logic, memory, and interconnect applications to enable novel computing and storage paradigms beyond the capabilities of conventional CMOS. The key idea is to utilize the properties of 2D material systems that are NON-EXISTENT in traditional 3D materials to achieve the performance or realize the novel functionalities that existing technologies are not able to offer. The center covers the following research vectors: material and device research, nanofabrication and advanced manufacturing processes, innovative metrology and characterization, and simulation and modeling.

CSME

The Center for a Secure Microelectronics Ecosystem (CSME) was launched with support from founding companies TSMC and Synopsys in conjunction with support through a U.S. Department of Defense (DoD)-funded workforce development program. CSME is co-directed by Professors Joerg Appenzeller and Anand Raghunathan. CSME is a first-of-its-kind global partnership of academia, industry, and government to advance research and workforce development in designing secure microelectronics. Its aim is to enable the creation of secure semiconductor chips and related products, from the foundry to the packaged system, based on a zero-trust model. CSME will provide advanced training opportunities to SCALE participants, while SCALE will support CSME through graduate traineeships, addressing the urgent need for engineering graduates with secure microelectronics skills.

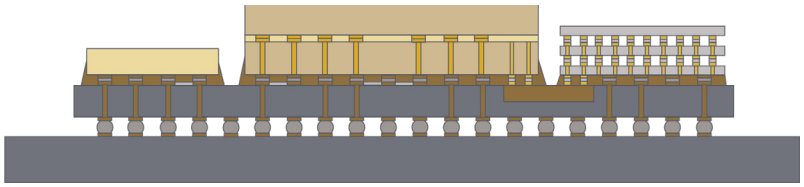


ICC

The Institute for Cognitive Computing aims to advance the field of cognitive computing through cross-layer innovation spanning brain-inspired computing models, algorithms, architecture, and hardware fabrics. The institute brings together faculty with diverse backgrounds to pursue these goals by facilitating collaborative research and training the next generation workforce in this critical domain.

CTRC

The Cooling Technologies Research Center (CTRC) is a graduated National Science Foundation Industry/University Cooperative Research Center and addresses pre-competitive, longer-term research and development issues in the area of high-performance heat removal from compact spaces.



ASIP

The Atalla Institute for Advanced System Integration and Packaging will address the challenges to research, "lab-to-fab" translation and workforce necessary to build the future microelectronic systems. The challenges include system architectural and physical design enabled by multiphysics modeling tools, high-density interposers and substrates, process development for interconnect pitch scaling, and thermal solution design, all while meeting the reliability and manufacturing yield goals. The ASIP institute will bring together integrated device manufacturers, fabless companies, EDA companies, equipment vendors, materials suppliers, OSATs, and university academics to develop advanced system integration and packaging solutions.

Research Excellence

Purdue research in semiconductors spans the "full stack" from materials and devices, to circuits, systems, and architecture.

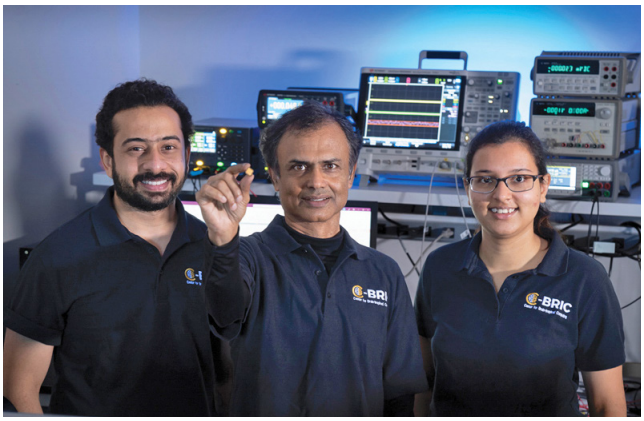
Advanced Packaging and Heterogeneous Integration

Co-directed by Professor Carol Handwerker and Professor Ganesh Subbarayan

Purdue is home to one of the nation's leading programs in advanced packaging and heterogeneous integration. Purdue co-leads the Semiconductor Research Corporation's Center for Heterogeneous Integration Research in Packaging (SRC CHIRP), the only advanced packaging center in the SRC portfolio. In addition, Purdue leads the SRC n-CORE NEW LIMITS: NEW materials for LogIc, Memory and InTerconnectS Center, co-funded by SRC members and NIST to develop synthesis, integration, and evaluation schemes for new BEOL materials for unique logic, memory, and interconnect applications to enable novel computing and storage paradigms beyond the capabilities of conventional CMOS. Complementing the above two SRC centers is the Cooling Technologies Research Center (CTRC), a graduated National Science Foundation Industry/University Cooperative Research Center (NSF/IUCRC), that has conducted leading-edge research on the thermal management of electronics for nearly 25 years. The Purdue team is addressing a critical research gap—the need to enable quick-turn, top-down packaged system development is an ability to automatically convert design intent into packaging strategy, materials selection, appropriate thermal solutions, and package circuit layout.

With a total of 24 faculty in advanced packaging across Purdue's College of Engineering, the Purdue team is focused on developing game-changing technologies such as electrical-thermal-mechanical deep co-design tools and techniques to translate design intent into automated package circuit layout. Specific research activities include Machine Learning (ML) assisted computational models that match multiphysics behavior of packages accurately, low power interconnects, advanced power-delivery solutions, innovative thermal solutions for die stack as well as package-level cooling, and advanced x-ray metrologies that enable real-time defect metrology, while also meeting the reliability and manufacturing yield goals so necessary for translating R&D to technology innovation. The goal of Purdue research is to enable a 50 times reduction in system realization time from architectural design to packaging.

Novel Approaches to Information Processing: Cognitive Computing



Co-directed by Professor Anand Raghunathan and Professor Kaushik Roy

The boundary between memory and processing that was drawn clearly in the early days of computing by von Neumann still defines virtually all modern computing platforms, but the gap between processor and memory speeds has grown to create the daunting "memory wall" that threatens to stymy further progress in computing system performance. Further, the energy cost of moving data between DRAM and processors in the roughly 100 million computer servers in the world exceeds the output of over two Hoover Dams! After decades of progress in computing systems, we must revisit the von Neumann paradigm. Professors Roy and Raghunathan lead research on new approaches to information processing in C-BRIC, the $36M SRC/DARPA Center for Brain-inspired Computing and in the Institute for Cognitive Computing. The goal is to deliver key advances in cognitive computing to enable a new generation of autonomous intelligent systems.

Cognitive computing brings together leading researchers from the fields of machine learning, computational neuroscience, theoretical computer science, neuromorphic hardware, distributed computing, and robotics and autonomous systems. Artificial Intelligence (AI) Hardware, another area of particular strength at Purdue, is also within the scope of the SRC/DARPA Center for Brain-inspired Computing. Eight faculty members from the School of ECE, with an ongoing search targeting two new hires, contribute to this effort. A major part of C-BRIC is focused on Compute-in-Memory (CiM) for efficient AI and data analytics. Computing-in-Memory (CiM) fundamentally blurs the distinction between processing and memory by bringing them closer, and in the extreme embedding processing capabilities within memory arrays. Besides radically improving the performance and energy efficiency of computing systems, CiM has the potential to enable entirely new categories of products and markets. Purdue researchers have pioneered several advances in the design of CiM systems and demonstrated them through tape outs of chips. A few of the recent tape outs include a 35.5 – 127.2 TOPS/W dynamic sparsity-aware reconfigurable-precision Compute-in-Memory SRAM macro for machine learning and a 65nm digital Compute-in-Memory Macro with fused weights and membrane potential for spike-based sequential learning tasks.

Atomic-Scale Engineering of Semiconductor Materials and Devices

Directed by Professor Peide Ye

Under the leadership of Professor Ye, Purdue faculty are actively engaged in the exploration of novel electronic materials and devices for post-Moore era semiconductor technologies. One of the utilized technologies is called atomic layer deposition (ALD). ALD is a thin-film deposition technique with atomic-scale controllable accuracy based on the sequential use of a self-limiting chemical process; it is a subclass of chemical vapor deposition. ALD became an enabling technology for the continuation of Moore's law by integrating high-k dielectrics in Si CMOS processes. ALD is a key process in fabricating semiconductor devices in particular as the dimension of state-of-the-art device technology is approaching single-digit nanometer length scales.

In the past decades, we have been working actively on ALD dielectrics and their integration on traditional and novel semiconducting channel materials including Si, Ge, III-V compound semiconductors, 2D materials, and oxide semiconductors. Beyond high-k and higher-k dielectrics, we also have explored ALD-grown ferroelectrics such as $HfZrO_2$ for emerging logic and memory applications (IEDM 2021). More recently, we pioneered the use of the ALD technique to form atomically thin oxide semiconductor channels with remarkable performance including unprecedented ultra-high drain currents and transconductances among all field-effect transistors based on any semiconductor materials (Nature Electronics 2022). ALD interlayers can also be used a phonon spectrum match buffer to enhance the thermal dissipation and electrical-thermal co-design of atomic-scale electronic devices.

Beyond graphene and transition metal dichalcogenides (TMDs) 2D materials research, Purdue faculty pioneered phosphorene (ACS Nano 2014) and tellurene (Nature Electronics 2018), two special elemental van der Waals 2D monolayers of phosphorus and tellurium with thickness less than one nanometer. We systematically studied their electrical, optical, thermal, and mechanical properties and their applications for electronic devices. More interestingly, we are able to form a single atomic chain of tellurium atoms towards the smallest semiconductor channel (Nature Electronics 2020).

These efforts are enabled by the Birck Nanotechnology Center, which is a state-of-the-art facility that allows atomic-scale nanomaterial synthesis and prototype atomic-scale fabrication and characterization.

Research Excellence *(cont'd)*

Novel Approaches to Information Processing: Probalistic Spin Logic

Directed by Professor Joerg Appenzeller, Professor Zhihong Chen, and Professor Supriyo Datta

Probabilistic Spin Logic (PSL) is a novel approach for information processing that is being explored by a team led by Professors Datta, Chen, and Appenzeller. The majority of today's digital circuitry is based on building blocks called bits that are deterministically 0 or 1. At the other end of the spectrum are quantum computers consisting of qubits which occupy some superposition of 0 and 1. The probabilistic-bit occupies a niche between these extremes, sharing qualities with both the classical-bit and the quantum-bit. The p-bit fluctuates probabilistically between 0 and 1, and can be pinned to one or the other state based on the magnitude and sign of its input. For a popular description see IEEE Spectrum at https://ieeexplore.ieee.org/abstract/document/9393992.

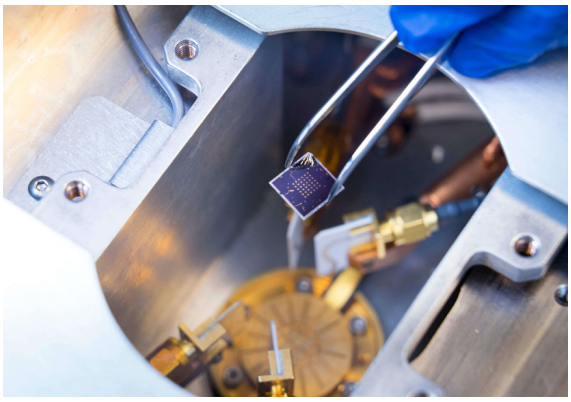
Just as a bit is only useful when in conjunction with other bits, p-bits can be correlated to form p-circuits. These circuits can be programmed to tackle a variety of problems that are often targeted by quantum computing, such as optimization, inferencing, and data encryption and decryption—without, however, the need for ultra-low temperatures. It is in the variety of applications, and the classical nature of the p-bit, that this building block comes to life, providing orders of magnitude improvement in performance (see Applied Physics Letters at https://aip.scitation.org/doi/full/10.1063/5.0067927) over standard CPU and GPU implementations.

To date the Purdue team has published many other breakthroughs (for an overview see https://ieeexplore.ieee.org/abstract/document/8995804), most notably an experimental demonstration of optimization and invertible logic using unstable magnetic tunneling junctions (MTJs), see Nature (https://www.nature.com/articles/s41586-019-1557-9), and the feasibility of MTJs to demonstrate that complex circuit operations are achievable in realistic hardware systems. This is particularly exciting because it demonstrates the feasibility of fabricating compact energy-efficient hardware p-bits by modifying existing magnetic random access memory (MRAM) technology.

For more information, see: https://www.purdue.edu/p-bit/.
To learn about a company commercializing this technology, see: https://ludwigcomputing.com/.

Emerging Logic, Memory, and Interconnect Technologies

Directed by Professor Muhammad Ashraf Alam, Professor Joerg Appenzeller, Professor Zhihong Chen, Professor David Janes, and Professor Peide Ye



Purdue Professors Alam, Appenzeller, Chen, Janes, and Ye are actively engaged in the exploration of emerging logic, memory, and interconnect technologies. Purdue's leadership is apparent from the support that these faculty receive from the Semiconductor Research Corporation (SRC) through center-level activities such as the nCORE NEW LIMITS Center (directed by Professor Chen) and JUMP, where Purdue PIs are involved in the ASCENT Center. In particular, these faculty have focused on experimental demonstrations of the above technologies based on novel materials including low-dimensional materials and ferroelectrics.

Professor Ye has been at the forefront of exploring novel materials for ferroelectric memory applications, and oxide-based channel materials such as In2O3 for back-end-of-line (BEOL) in-memory computing that requires transistors with ultra-low standby power specs and high on-current capabilities. Professor Ye has worked in strong collaboration with Professor Alam, who focuses on the reliability physics of these unexplored novel active device elements.

Professors Chen and Appenzeller have experimentally demonstrated that novel low-dimensional materials such as transition metal dichalcogenides (TMDs) with body thickness less than one nanometer can be utilized as channel materials in ultra-high performance transistors and offer performance beyond what silicon technologies can offer. Their work highlights the excellent scalability of devices from TMDs for the next generations of logic computing units (https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9372049). The same sub-1nm thickness also proved highly promising for the use of TMDs as diffusion barriers in future back-end-of-line (BEOL) interconnect technologies (https://aip.scitation.org/doi/10.1063/5.0013737). Professors Chen and Appenzeller also observed that MoTe2 (a member of the TMD family) based memories give rise to a novel type of phase change switching that is controlled by electric fields. This is a low-power, fast switching memory that combines the characteristics of resistive random access memories (RRAM) and phase change memories (PCM) (https://www.nature.com/articles/s41563-018-0234-y).

These efforts on emerging technologies are enabled by the Birck Nanotechnology Center, which is a state-of-the-art facility that allows prototype fabrication and characterization at scale.

Reliability of Semiconductor Logic and Memory Devices

Directed by Professor Muhammad Ashraf Alam

Under the leadership of Professor Alam, Purdue is well-known for fundamental work on the reliability physics of semiconductor logic and memory devices, both for application-specific consumer electronics and radiation-hardened secure electronics for defense applications. A variety of test equipment available at the Birck Center would support the development of new performance/reliability characterization techniques for DRAM and Flash memories.

It is well known that bit errors (and "repeated-read" security failures) increase significantly as DRAM transistors are scaled below 28-32 nm node because the stored charge at the capacitor node and the leakage through the access transistor are sensitive to transistor scaling. Radiation- induced charge loss and SILC-related gate leakage are concerns that must be addressed. Similarly, next-generation 3D NAND Flash memories will continue to grapple with read-margin, retention, and endurance issues arising from: (a) the threshold-voltage variation due to ambient temperature-sensitivity of polysilicon channel mobility, (b) threshold-voltage fluctuation due to trapping/de-trapping in the tunnel oxides, and (c) the reduced channel cross-section and enhanced field making the bottom cells susceptible to correlated HCI, TDDB, and radiation damages. There is an opportunity to develop a more efficient ECC because the bit-flips in 3D NAND Flash are likely to be correlated. Further, for the Compute-in-Memory (CiM) applications involving both logic and memory transistors, classical ECC may not be relevant.

In short, Purdue can support the development of new characterization techniques and physics-based reliability models for HCI, SILC, TDDB, and radiation-related reliability issues of DRAM and Flash memories. These reliability models will be informed by a deep understanding of the cross-layer design considerations, including those arising from heterogeneous integration (HI) that defines the thermal and stress-related cross-talk among various components.

Research Excellence *(cont'd)*

Sustainability of Electronic Ecosystems

Directed by Professor Carol Handwerker

Sustainability is a core value at Purdue, as evidenced not only in green buildings and clean energy, but also in creating technologies that make the world a better place. Under the leadership of Professor Handwerker, Purdue is committed to the "Double Bottom Line" to care for people and the planet through the development of new technologies.

Purdue has a strong tradition in quantifying the economic, environmental, and societal impacts of the decisions made in early-stage R&D on the ultimate impacts in the realized products and their global supply chains. We welcome collaborations in coupling sustainability R&D at Purdue with the supply chains, technology developers, and decision-makers of companies. Three examples of recent collaborations that could serve as models are:

1. DOE Critical Materials Hub in which Purdue provides quantification of both commercialization potential and environmental impact of technologies being developed by researchers from four DOE Labs, ten companies, and eight universities;
2. iNEMI Project on Value Recovery from End-of-Life Electronics, co-led by Purdue, in which Seagate, Google, Microsoft, Cisco, and others demonstrated nine circular economy technologies for remanufacturing, reuse, and recovery of rare earth magnets in hard drives; and
3. NSF graduate education and training program on Design for Globally Sustainable Electronics in which DBL is a central tenet, with a customizable curriculum based on partner company needs. For the latter, these courses are part of the new MS in Semiconductors and Microelectronics at Purdue and the undergraduate certificate in Semiconductors.

Finally, Purdue not only has deep expertise in R&D but also in workforce development to address issues of local, regional, and global concern, including but not limited to clean energy, smart grids, system design and operation for Net Zero, and developing leadership for creating and operating sustainable systems.

High Frequency Electronics

Purdue University is a pacesetter in High-frequency Electronics, also referred to as Radio Frequency (RF) Engineering. There are more than 12 faculty members and 100 PhD students, postdocs, and research scientists that lead major centers/projects spanning the sub-GHz to the millimeter-wave space. In addition to Birck Nanotechnology Center facilities, RF researchers utilize more than 10,000 square feet in the Elmore Family School of Electrical and Computer Engineering to design and characterize devices up to 220 GHz. Recent breakthroughs include:

- PiezoMEMS resonant actuators from 100 MHz to 50 GHz for LIDAR, microwave-to-optical quantum coherent converters, and mechanical control of color center defects in Diamond and Silicon Carbide (Bhave).
- Low-noise RF front-ends, online adaptive calibration schemes, and massive sensor data processing. The team demonstrated the first electromagnetic tracking system with an unprecedented level of accuracy and a non-invasive current monitoring system with world record SNR (Jung).
- Multi-functional RF filter architectures in the 1-100 GHz range. Examples include supercavity resonators, automatically tunable filters, and all-silicon tunable filters. Moreover, we have demonstrated the first switchable on-chip silicon plasma devices and antennas such as K-band silicon monopoles, plasma-switch impedance tuners, and DC-110 GHz plasma silicon switches (Peroulis).
- Adaptive sub-6 GHz and non-radiative Covert Communication (kHz-GHz) Integrated Circuits and Systems. We demonstrated the first physically secure Electro-Quasistatic Communication on Human Body and other conductors with 100x lower energy than Bluetooth. EM-Security which includes first ultra-resilient circuit-level EM-Side Channel Protection, RF-PUF, RF-PSF and EM-emanation detection. Also, we work on EM based Biosensors and application of RF/EM Sensing and Communication in Internet of Bodies (Sen).
- Photonically-enabled RF arbitrary waveform generation, including application to high range resolution W-band radar, RF photonic down-converters for use in sampling broadband electronic signals, interferometric direction-finding and signal characterization architectures for wideband sensing, and optical frequency combs for coherent links between RF and optical frequencies (Weiner, McKinney).
- Fast and efficient math/physics-based modeling of highly complex RF structures resulting in greatly reduced computer time (Chew).

https://tinyurl.com/WangHallLabs

Faculty

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Hadiseh Alaeian Assistant Professor, Electrical and Computer Engineering and Physics and Astronomy					●			
Muhammad Ashraf Alam Jai N. Gupta Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
Joerg Appenzeller Scientific Director of Nanoelectronics, Birck Nanotechnology Center; Barry M. and Patricia L. Epstein Professor, Elmore Family School of Electrical and Computer Engineering					●			
Santokh Badesha Distinguished Professor of Electrical and Computer Engineering					●			
Shubhra Bansal Associate Professor, School of Mechanical Engineering					●			
Thomas Beechem Associate Professor, School of Mechanical Engineering					●			
Peter Bermel Director of SCALE; Associate Director of Graduate Admissions; Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering					●	●	●	
Sunil Bhave Associate Director of Operations, Birck Nanotechnology Center; Professor, Elmore Family School of Electrical and Computer Engineering		●	●	●	●			

*Other Areas: ■ Simulation and Modeling ◆ Manufacturing System Design and Optimization ⬢ Digital Manufacturing ⬟ Resilient Supply Chains and Risk Analysis

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Stephan Biller Director of Dauch Center for the Management of Manufacturing Enterprises; Harold T. Amrine Distinguished Professor, School of Industrial Engineering and Mitchell E. Daniels, Jr. School of Business								⬢ ◆ ⬟
John Blendell Professor, School of Materials Engineering	●							
Alexandra (Sasha) Boltasseva Ron and Dotty Garvin Tonjes Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
Michael Capano Professor, Electrical and Computer Engineering					●			
Srinivasan Chandrasekar Professor, Industrial Engineering and Materials Engineering (by courtesy)					●		●	
Nikhilesh Chawla Ransburg Professor, School of Materials Engineering; Associate Dean for Engineering in Indianapolis	●							
Yong Chen Karl Lark-Horovitz Professor, Physics and Astronomy					●			
Zhihong Chen Mary Jo and Robert L. Kirk Director, Birck Nanotechnology Center; Reilly Professor, Elmore Family School of Electrical and Computer Engineering					●			
Gary Cheng Professor, Industrial Engineering	●				●			

*Other Areas: ■ Simulation and Modeling ⬢ Digital Manufacturing ◆ Manufacturing System Design and Optimization ⬟ Resilient Supply Chains and Risk Analysis

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Weng Chew Distinguished Professor, Electrical and Computer Engineering		●						
Supriyo Datta Thomas Duncan Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
Daniel Elliott Professor, Electrical and Computer Engineering and Physics					●			
Edwin García Professor, School of Materials Engineering								■
James Gibert Associate Professor, Mechanical Engineering	●							
Ana María Estrada Gómez Assistant Professor, Industrial Engineering								■ ⬢ ◆ ⬟
Luis Gomez Assistant Professor, Electrical and Computer Engineering		●						
Ronald Goossens Adjunct Professor					●			■
Ananth Grama Samuel D. Conte Professor, Computer Science							●	

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Jeffery Gray Associate Professor, Electrical and Computer Engineering					●			
Sumeet Gupta Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering			●					
Carol Handwerker Reinhardt Schuhmann, Jr. Distinguished Professor, School of Materials Engineering	●						●	
Mahdi Hosseini Assistant Professor, Elmore Family School of Electrical and Computer Engineering				●	●			
John Howarter Associate Professor, School of Materials Engineering and Environmental and Ecological Engineering	●							
Inez Hua Professor, School of Civil Engineering and Environmental and Ecological Engineering							●	
Muhammad Hussain Professor, Elmore Family School of Electrical and Computer Engineering					●			
Zubin Jacob Elmore Professor, Electrical and Computer Engineering					●			
David Janes Professor, Elmore Family School of Electrical and Computer Engineering					●			

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Dan Jiao Synopsys Professor, Elmore Family School of Electrical and Computer Engineering		●						■
David Johnson Associate Professor, Industrial Engineering; Joint Appointment with Political Science							●	
Alexander Kildishev Professor, Electrical and Computer Engineering		●						
Gerhard Klimeck Director of the Network for Computational Nanotechnology; Reilly Director of the Center for Predictive Materials and Devices; and Elmore Professor, Elmore Family School of Electrical and Computer Engineering					●	●		
Cheng-Kok Koh Professor, Electrical and Computer Engineering			●					
Marisol Koslowski Associate Dean for Global Engineering Programs and Partnerships; Professor, School of Mechanical Engineering								■
Tillmann Kubis Katherine Ngai Pesic and Silvaco Associate Professor, Elmore Family School of Electrical and Computer Engineering					●			■
Seokcheon Lee Professor, Industrial Engineering								■ ⬢ ◆ ⬟
Haitong Li Assistant Professor, Elmore Family School of Electrical and Computer Engineering			●		●			

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Yung-Hsiang Lu Professor, Electrical and Computer Engineering			●					
Mark Lundstrom Senior Advisor to the President; Chief Semiconductor Officer; Don and Carol Scifres Distinguished Professor, Elmore Family School of Electrical and Computer Engineering					●			
Mike Manfra Scientific Director, Microsoft Quantum Lab Purdue; Bill and Dee O'Brien Distinguished Professor, Physics and Astronomy; and Professor, Elmore Family School of Electrical and Computer Engineering and School of Materials Engineering					●			
Amy Marconnet Associate Professor, School of Mechanical Engineering	●							
Jason McKinney Associate Professor, Electrical and Computer Engineering		●						
Michael Melloch Associate Head and Professor, Electrical and Computer Engineering					●			
Saeed Mohammadi Professor, Elmore Family School of Electrical and Computer Engineering		●	●		●			
Issam Mudawar Betty Ruth and Milton B. Hollander Family Professor, School of Mechanical Engineering					●			
Evgenii Narimanov Elmore Professor, Electrical and Computer Engineering					●			

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Shimon Nof Director, PRISM Center; Professor, Industrial Engineering							●	■
Liang Pan Associate Professor, School of Mechanical Engineering	●							
Dimitrios Peroulis Senior Vice President for Partnerships and Online, Reilly Professor of Electrical and Computer Engineering		●	●	●	●			
Irith Pomeranz Cadence Professor, Electrical and Computer Engineering			●					
Nagabhushana Prabhu Professor, Industrial Engineering					●			■ ⬢ ◆ ⬟
Minghao Qi Professor, Elmore Family School of Electrical and Computer Engineering				●	●			
Anand Raghunathan Silicon Valley Professor of Electrical and Computer Engineering, Elmore Family School of Electrical and Computer Engineering			●					
Vijay Raghunathan Vice President for Global Partnerships and Programs; Director of Semiconductor Education; Professor of Electrical and Computer Engineering, Elmore Family School of Electrical and Computer Engineering			●					
Rahim Rahimi Assistant Professor, School of Materials Engineering						●		

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Thomas Roth Assistant Professor, Electrical and Computer Engineering		●						
Kaushik Roy Director, Center for Brain-Inspired Computing, a DARPA/SRC JUMP Center; Edward G. Tiedemann Jr. Distinguished Professor, Elmore Family School of Electrical and Computer Engineering			●		●			
Xiulin Ruan Director of Graduate Recruitment and Admissions and Professor, Mechanical Engineering								■
Siva Seetharaman Assistant Professor, Industrial Engineering	●			●	●			■ ◆ ⬟
Shreyas Sen Elmore Associate Professor, Elmore Family School of Electrical and Computer Engineering and Biomedical Engineering		●	●					
Ali Shakouri Associate Dean, Research and Innovation; Professor, Elmore Family School of Electrical and Computer Engineering					●	●		
Vladimir Shalaev Bob and Anne Burnett Distinguished Professor, Electrical and Computer Engineering					●			
Yu She Assistant Professor, Industrial Engineering					●	●		■ ⬢ ◆
Young-Jun Son James J. Solberg Head and Ransburg Professor, School of Industrial Engineering					●			■ ⬢ ◆ ⬟

Faculty *(cont'd)*

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Ganesh Subbarayan Co-director, SRC Center for Heterogeneous Integration Research in Packaging *(CHIRP)*; James G. Dwyer Professor, Mechanical Engineering	●						●	■
John Sutherland Fehsenfeld Family Head, School of Environmental and Ecological Engineering							●	
Pramey Upadhyaya Assistant Professor, Elmore Family School of Electrical and Computer Engineering					●			
Juan Wachs Professor, Industrial Engineering					●			■
Haiyan Wang Basil S. Turner Professor, Elmore Family School of Electrical and Computer Engineering and School of Materials Engineering					●			
Kevin Webb Professor, Elmore Family School of Electrical and Computer Engineering					●			
Tiwei Wei Assistant Professor, School of Mechanical Engineering	●							
Dana Weinstein Professor, Elmore Family School of Electrical and Computer Engineering		●	●	●	●			
Justin Weibel Associate Professor, School of Mechanical Engineering	●							

Faculty Name, Title, and Department	RESEARCH AREAS							
	Heterogeneous Integration and Advanced Packing	High-Frequency Electronics	Integrated Circuits and Systems Design	MEMS and Photonics	New Devices, Materials, and Fabrication	Sensors and Thermal Imaging	Sustainability and Life Cycle Analysis	Other Areas*
Wenzhuo Wu Ravi and Eleanor Talwar Rising Star Professor, Industrial Engineering	●	●	●	●	●	●		■
Dongyan Xu Samuel D. Conte Professor of Computer Science; Director of CERIAS; and Assistant Professor, Purdue Polytechnic Institute							●	
Xianfan Xu James J. and Carol L. Shuttleworth Professor, School of Mechanical Engineering, Professor, Elmore Family School Electrical and Computer Engineering (by courtesy)				●	●			
Peide (Peter) Ye Richard J. and Mary Jo Schwartz Professor, Elmore Family School of Electrical and Computer Engineering					●			
Yuehwern Yih Director, Smart Systems and Operations Laboratory; Director, USAID LASER PULSE; Tompkins Professor, Industrial Engineering	●							■ ⬢ ◆ ⬟
Xinghang Zhang Professor, School of Materials Engineering	●							
Fu Zhao Professor, School of Mechanical Engineering and Environmental and Ecological Engineering							●	

PURDUE UNIVERSITY

Semiconductors@Purdue in the News

The Economist

August 5, 2023

America is Building Chip Factories. Now to Find the Workers

"Leading the charge is Purdue University in Indiana, which last year launched a semiconductor degree programme for both undergraduates and graduates. The explicit aim of Purdue's 'lab-to-fab' model is to collaborate more closely with companies."

The New York Times

August 6, 2023

Indiana Tests if the Heartland can Transform into a Chip Hub

"Some of the work paid off. When Indiana beat out four other states for SkyWater's $1.8 billion chip facility, the company said it was impressed by the coordination between state leaders and Purdue's new president, Mung Chiang, who launched the nation's first semiconductor degree programs to nurture workers for chip makers."

THE WALL STREET JOURNAL.

April 11, 2024

America's Chip Renaissance Needs Workers

"South Korea announced it would partner with Purdue University on a $3.9 billion semiconductor complex here, the largest single corporate investment in state history."

NBC NEWS

August 9, 2024

Two Years Since the CHIPS Act, the Race Heats up to Train Tens of Thousands of Workers

"A Purdue University program [Summer Training on Awareness and Readiness for Semiconductor–STARS] just finished its second year prepping undergrads for chipmaking jobs, including at a nearby plant set to start mass production soon after they graduate. [...] STARS will 'definitely prepare me and give me the good experience for future opportunities,' said Robert Zhang. The rising sophomore at Purdue University participated in the school's STARS program, an eight-week intensive program that wrapped up its second summer last month with 100 students, up from around 70 initially."

Semiconductors@Purdue 2022-2024

Purdue President Mung Chiang sits with Intel CEO Patrick Gelsinger at a Fireside Chat on October 17th, 2023 at Purdue University.

Birck Nanotechnology Research Scientist, Angshuman Deka works with middle school students at the 2023 JA JobSpark Convention in Indianapolis, September 2023.

Purdue President Mung Chiang with President Joe Biden at the G7 Summit in Japan, May 2023.

Purdue President Mung Chiang with Secretary of Commerce Gina Raimondo on her visit to Purdue University's campus in September 2022.

Brian Dunlap, Vice President of 300mm Fab Operations at Texas Instruments, speaking to students at the 2023 Semiconductor Info Session in September 2023.

Purdue President Mung Chiang at the G7 Summit in Hiroshima, Japan establishing the "UPWARDS Network." The agreement was signed in the presence of, among others, U.S. Secretary of State Antony Blinken; Japan's Minister for Education, Culture, Sports, Science and Technology Keiko Nagaoka; and U.S. Ambassador to Japan Rahm Emanuel.

Purdue University: Silicon Heart of America

SK hynix Facility for AI Memory Chips in West Lafayette Marks the Largest Single Economic Development in the History of Indiana

SK hynix Inc. announced on April 3th, 2024, that it plans to invest close to $4 billion to build an advanced packaging fabrication and R&D facility for AI products in the Purdue Research Park. This development of a critical link in the U.S. semiconductor supply chain in West Lafayette marks a giant leap forward in the industry and the state and is expected to provide more than a thousand new employment opportunities in the Greater Lafayette community. The company plans to begin mass production in the second half of 2028.

Purdue Faculty Serving in National Semiconductor Leadership Roles

Carol Handwerker

Reinhardt Schuhmann Jr. Professor of Materials Engineering, Environmental and Ecological Engineering, Purdue University | Industrial Advisory Committee Member

Dr. Handwerker currently serves as the Reinhardt Schuhmann Jr. Professor of Materials Engineering, Environmental and Ecological Engineering at Purdue University. She formerly worked at NIST, where she became chief of the Metallurgy Division. She is well-known for her research on determining the best options for solder that connect electronic components to circuit boards, focusing on almost any physical condition that a circuit board could encounter. Her current research is part of the U.S. Partnership for Assured Electronics (USPAE) and is backed by a $40 million U.S. Department of Defense contract. Her work on the committee, alongside three other representatives from academia, is to provide guidance to the federal government in relation to the recently passed CHIPS and Science Act, which has appropriated $52 billion toward bolstering the semiconductor industry in the United States. Dr. Handwerker has been appointed to serve as a member of the Industrial Advisory Committee with the National Institute of Standards and Technology in as of June 2023.

Dana Weinstein

Professor, Electrical and Computer Engineering, Purdue University | Special Advisor in CHIPS R&D, Industry Innovation, White House Office of Science and Technology

Dr. Weinstein is a Professor in Purdue's School of Electrical and Computer Engineering. Prior to joining Purdue in 2015, Dr. Weinstein joined the Department of Electrical Engineering and Computer Science at MIT as an Assistant Professor and served as an Associate Professor there between 2013 and 2015. She is a Purdue Faculty Scholar, and a recipient of the NSF CAREER Award, the DARPA Young Faculty Award, the first Intel Early Career Award, the first TRF Transducers Early Career Award, and the IEEE IEDM Roger A. Haken Best Paper Award. Dr. Weinstein's current research focuses on innovative microelectromechanical devices for applications ranging from MEMS-IC wireless communications, clocking, and sensing to micro-robotic actuators and flexible substrate ultrasonic transducers. Dr. Weinstein has been appointed to serve as a Special Advisor for CHIPS R&D, Industry Innovation at the White House Office of Science and Technology as of December 2023.

2024 READI High School Program and STARS Program faculty, staff, and students. (Photo: Vincent Walter)

CHIP rendering of the Purdue Campus | Take a quick tour!

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